Lecture 1.
Mixed-Signal Design & Automation
-- An Introduction

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Outline

- Course outline
- Mixed-signal design
- Analog/mixed-signal (AMS) design automation
- Analog synthesis – state-of-the-art
- System-level mixed-signal design

Mixed-Signal Design

- **Circuits containing both continuous- and discrete-time signal processing (SP) components**
- **Requiring design skills in both analog and digital domains**
  - **AD/DA converters (in particular $\Sigma\Delta$ modulator)**
  - **Sampling circuits**
  - **Switched-Capacitor (SC) filters (discrete-time SP)**
  - **Amplifiers (in particular opamps)**
  - **Realization of DSP theory**
  - **Digital calibration (digitally control analog accuracy)**
- **Nowadays over 80% of the design effort for a chip is spent on the analog part plus system-level integration.**

Features of Mixed-Signal Design

- "Analog design" @ the core
- Knowledgeable on DSP
- Skillful use of description language beyond SPICE
  - Verilog-AMS, ...
  - Matlab/Simulink
  - Other Math Tools
- Good knowledge on latest IP
- Full of design innovation
- Fabrication support
- Difficulty in testing

Course Motivation

- **This is a research oriented course**
  - **The design automation level of analog/mixed-signal design is still very low!**
  - **People are using self-customized design methodology**
  - **rather than EDA-tool defined standard design methodology**
  - **So far labor work dominant**

- **So most of the mixed-signal design process is slow, trouble plagued, hard to catch up schedule.**

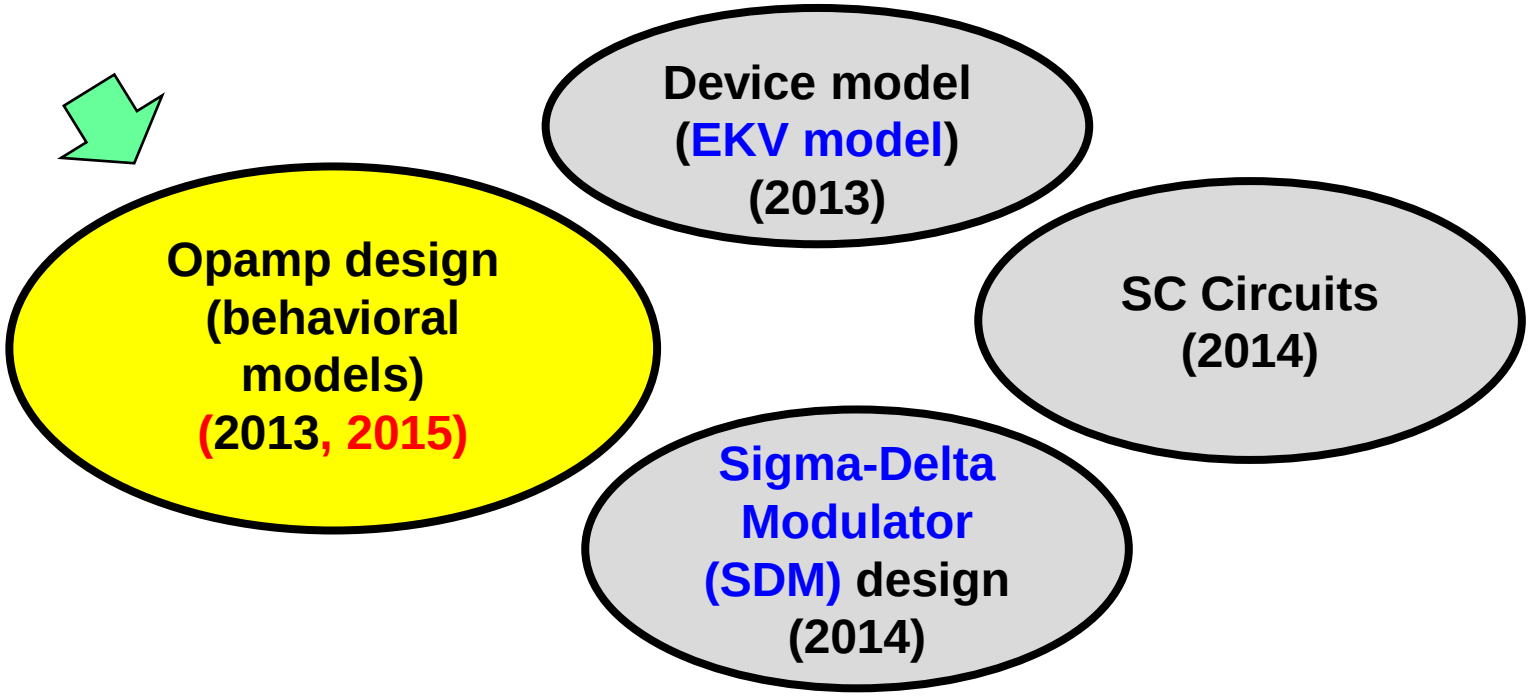
- **In the past years we have produced some unique research results on AMS design automation.**

Course Goals

- **Introduce some unique design techniques by case study and analysis**
- **Will be focused on**
  - **most common circuit blocks (opamps, SC circuits, etc.)**
  - **special but effective circuit analysis techniques**
  - **widely used behavioral modeling techniques for simulation**

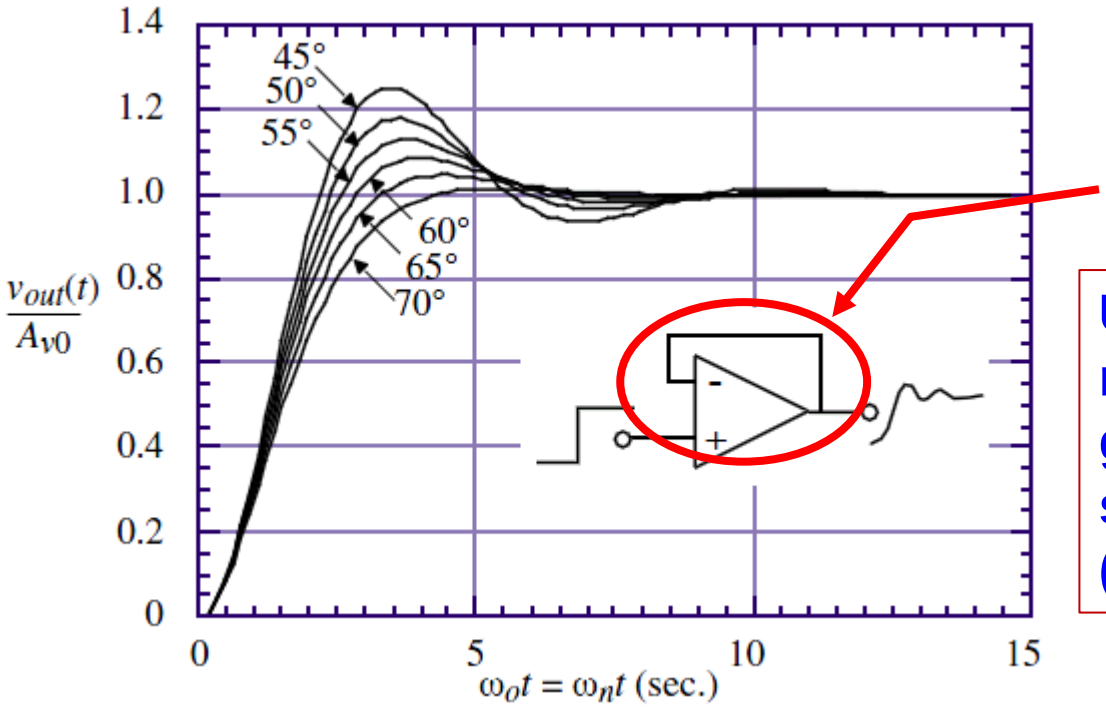
- **Course materials are collected from a variety of courses offered worldwide by some distinguished professors**

Course Coverage (this year)



- **The course contents vary over the years but with enhancements.**
- **Emphasizing**
  - **Non-ideal analysis; circuit imperfections**
  - **Behavioral modeling and system-level issues**

Example: Modeling large-signal response



Using a simple model to generate large-signal response (slew & settling)

- **To achieve "fast" step response we need to know what part of circuit affect settling / phase margin the most.**
- **How to quickly size MOSFET devices**
- **How is the circuit susceptive to circuit variation, parasitics, etc. ...**

Expectation on Student's Background

Students coming to this course should

- **know basic analog IC design**
- **knowledgeable in DSP theory & circuits**
- **have entry-level programming skills: MATLAB, C/C++, etc.**

- **Students working in the areas of analog, RF, bio-medical circuits, or even high-speed digital circuits are welcome.**

Will assign course projects ...

- **I will assign course projects according to the students' background and working research area.**

- **Optional subjects:**
  - **Circuit design (circuit + EDA tools)**
  - **Develop models (circuit + software)**
  - **Writing design tool (software)**

Course Grading (Tentative)

- **Occasional homework – 20%**
  - **Exercising on circuit analysis skills**
- **Course projects (2) – 30% x 2**
  - **Optional projects**
  - **Background introduced in lectures**
  - **will divide into modules: "proposal, seminar, project report"**
- **In-class seminar is encouraged – 20%**
  - **Students are required to present project progress**
- **No exam**

Topics Covered Before (2013, 2014)

(Year 2013)

- Device (EKV Model)
- Charge Sheet Model
- gm/ID Method
- Opamp Design Basics
- DPI/SFG Method
- Pole/zero analysis of two-stage opamps
- Opamp sizing method (traditional)

(Year 2014 – emphasizing discrete-time signal processing)

- ADC overview
- SC Device Basics
- SC circuit analysis basic/advanced
- SC HSPICE simulation
- Sigma-Delta ADC basics
- DPI/SFG method
- Sigma-Delta Modulator
- Two-stage amplifier pole/zero analysis
- SDM behavioral simulation

Topics Covered this Semester (Fall 2015)

- **Will mainly focus on "opamp" design, analysis, and modeling**
- **Detailed analysis on some less well known designs, such as**
  - **Detailed slew and setting analysis and modeling**
  - **Different opamp topologies and analysis**
- **DPI/SFG method (an easy-to-learn, easy-to-use hand calculation method for small-signal analysis)**

- **Touching some design automation issues**
  - **Definitely requiring EDA skills (algorithms + software)**

Many Arising Needs Recently

- **Low-power design for nodes in wireless sensor network (WSN)**
- **Low-frequency but high fidelity design in biomedical circuits**
- **Near-threshold / subthreshold design for low power**
- **Not always high-performance / high-speed design like in wireless communication applications (getting mature)**

Low amplitude (weak signal)

Low frequency (slow signal)

Table 1: Bio-Potential Signals

Signal	Amplitude(μv)	Frequency(HZ)
ECG	1000-5000	0.5-150
EEG	10-50	0.1-100
EMG	50-5000	10-1000
EOG	10-100	DC-10

Electrocardiogram (ECG), electroencephalogram (EEG), electromyogram (EMG)

Mixed-Signal Design (MSD)
- Issues, Challenges, and State-of the-Art for Automation

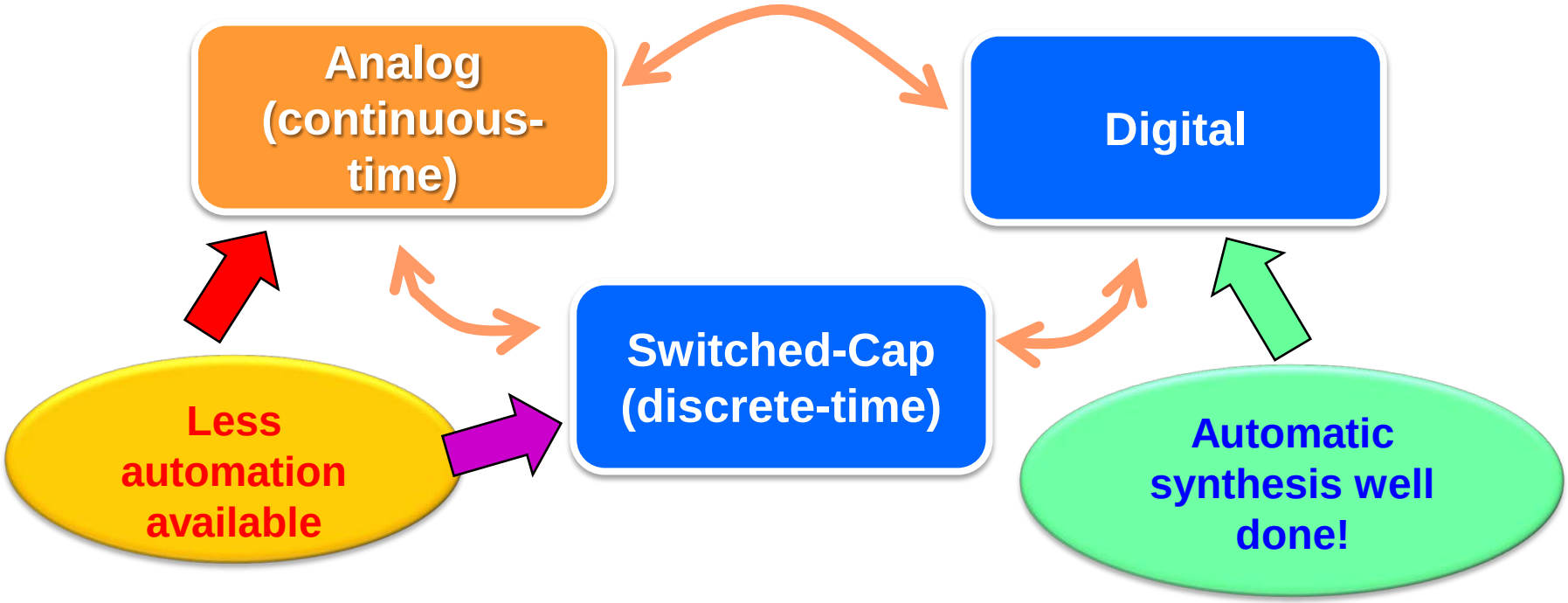
Mixed-Signal Circuits in SoC

- **Today 70% + SoC products have mixed-signal circuits**

Examples:

- **Phase-locked loops (PLL) - analog / digital**
- **DC-DC converter (power management)**
- **Analog/digital interfacing circuits**
- **RF front-ends (LNA, LO, VCO, ADC)**
- **Sensor**
- **Implantable devices**
- **...**

Automatic Synthesis – State-of-the-Art



- Design automation of the whole system is not there yet
- Need behavioral description of each part
- Analog design still quite manual today!
- Gradually moving toward IP-based design & service

Mixed-Signal Design Style

- "Top-down" design is in mainstream for digital-domain.
  - From "description" to "physical implementation"
- However, AMS design is not purely "top-down" yet, some blocks has to be "bottom-up"
  - Like transistor-level design of opamp;
  - Circuit topology design cannot be top-down
- Pure "top-down" design in analog domain would have to rely on mature IP support
  - Offering predesigned analog block library;
  - e.g., Cadence P-Cell (schematic to layout)
  - Mature silicon verification technology
- EDA tool support is still weak today.

Challenges

- **Reduced supply voltage in advanced process nodes benefits digital design (although leakage worsens)**
- **But does not benefit analog design a lot because of**
  - **shrinking headroom (reduced signal range)**
  - **reduced noise margin;**
  - **worsened process variation (increased matching error)**

- **Consequence: more complicated circuit has to be designed to cope with these challenges**
  - **complicated circuit**
  - **increases power and area budget**
  - **increases noise**
  - **reduces reliability**

Device Issues

- **Most library transistors are only optimized for digital domain;**
  - **but weakly for analog domain**
  - **matching, noise, etc.**

- **Capacitors and resistors are treated as parasitics in digital domain,**
  - **but they are design parameters in analog domain,**

- **Cap/Res in analog circuit occupy large area (5~10 x)**
- **Parasitic effects are more concerned in analog domain**

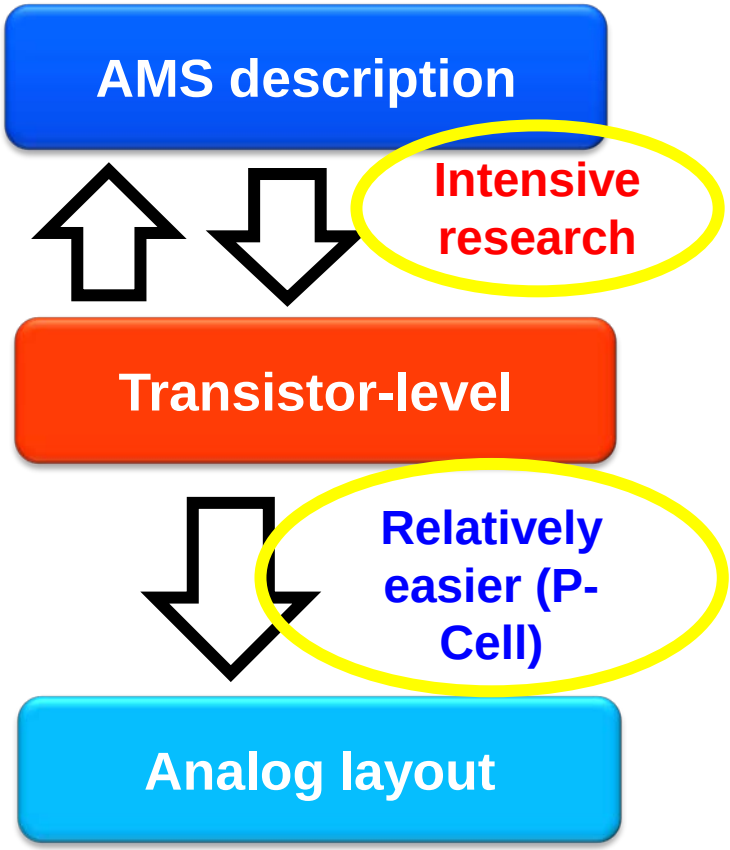
Technology Portability

- **Circuits designed in an older CMOS process may not function properly in a new generation process**

- **Analog IPs must seek process-independent design using the P-Cell tool/technology**

Challenges to Analog CAD

- **Circuit implementation:** "behavioral description" ➔ "transistor circuit"
- **Behavioral modeling**: "transistor circuit" ➔"behavioral description"
- Translation back and forth btw **"behavioral-level"** and **"transistor-level"** **(completely different from "digital" domain)**



Behavioral Modeling

- **Developing behavioral models is quite an art.**
- **Requiring cross-domain knowledge:**
  - **to understand circuit details;**
  - **to predict technology evolution and variation;**
  - **to create behavioral models that would work in different operation domains (time, frequency, distortion, ...)**

- **Designers hope to have good automation tools to facilitate "behavioral modeling".**

- **This work remains "incomplete" because there are so many different analog modules**
  - **and their design keeps evolving**

Mixed-Signal Design Issues

Requiring good sense of process

Analog design requires device & process knowledge:

- **Extremely thin gate oxide**
  - **1.5 – 2.2 nm for 130nm node**
  - **1.1 – 1.7 nm for 90nm node**
- **Shallow source and drain diffusions**
- **Shallow trench isolation (STI)**
- **Multiple oxide thicknesses (C_{ox})**
- **Multiple threshold voltages (V_{th})**
- **Gate-induced drain leakage (GIDL)**
- **Near threshold phenomena**

we wish to have simpler device models to manage all these ...

Requiring cross-level simulations

- **Most circuit simulators are dedicated to specific levels, like SPICE for transistor-level simulation, but hard to use it for system-level simulation.**
- **Buying a fully functional tool chain is expensive.**
  - **Only some leading design companies can afford**
- **Simulations at different levels would require different accuracy control and optional settings, which is highly skill-driven.**
- **Circuit sizing of mixed-signal systems remains a big challenge (simulation could take hours and days).**

Full Automation = Synthesis

Synthesis in Digital Domain

- **From mid-1980s: Commercialized logic synthesis tools (Synopsys/ Cadence)**
  - **Description-based synthesis flow**
    - **RTL description**
    - **➔ gate-level netlist**
    - **➔ physical (GDSII)**
    - **➔ post-layout verification**
    - **design constraints (Timing/Power/Area).**
  - **Fully logic compilation + timing**
  - **Interconnect timing model embedded in tool**
  - **Now, IP reuse & SoC design have been state-of-the-art**

Analog Synthesis

- **Much more challenging!**
- **One stage to another is not logic translation; requiring guarantee of accuracy in real values.**
- **Design targets and constraints are nonlinear functions of circuit components:**
  - **jitter, offset, slew rate (SR),**
  - **input/output impedance,**
  - **pole/zero, gain, phase margin, stability,**
  - **power, noise, distortion, and so on,**
- **Optimization is multi-variable and highly nonlinear!**
  - **Sizing & biasing are topology dependent**
  - **Continuous-variable with high-dimensional search space**
- **Circuit performance depends on custom layout**

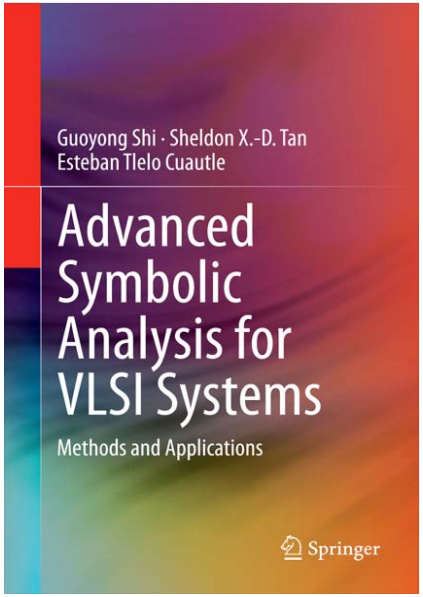
Challenges

- **Synthesis requires multi-objective optimization (e.g., opamp)**
  - **Gain**
  - **Bandwidth**
  - **Phase margin / gain margin**
  - **Slew rate (SR)**
  - **Common Mode Rejection Ratio (CMRR)**
  - **Power Supply Rejection Ratio (PSRR)**
  - **Distortion, noise**
  - **...**
- **All depending on device and circuit topology details**
- **Many design goals are conflicting**

Symbolic Approach

- **Symbolic methods enable "automatically" analyzing circuit blocks**
- **Equation-based automatic generation can partly incorporate expert knowledge**
- **Capable of generating performance metrics in device parametrics**
- **and even circuit topology**

- **Enables more efficient design space exploration**
- **Mostly current research subjects**



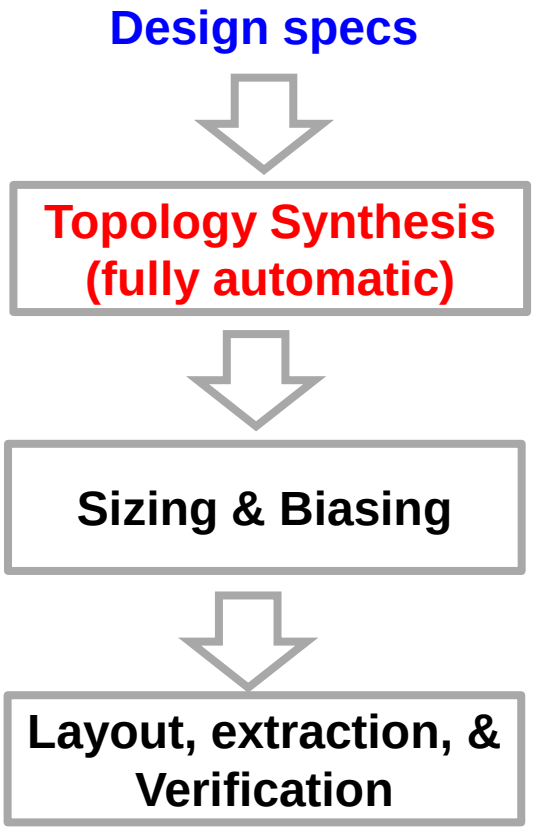
Analog Design Inputs

- **Behavioral AMS description**
- **Transistor-level SPICE netlist**
  - **Hand-written or generated by a schematic editor**
- **Test benches**
  - ***Stimulus signals*** **and expected** ***responses***
- **Design specs**

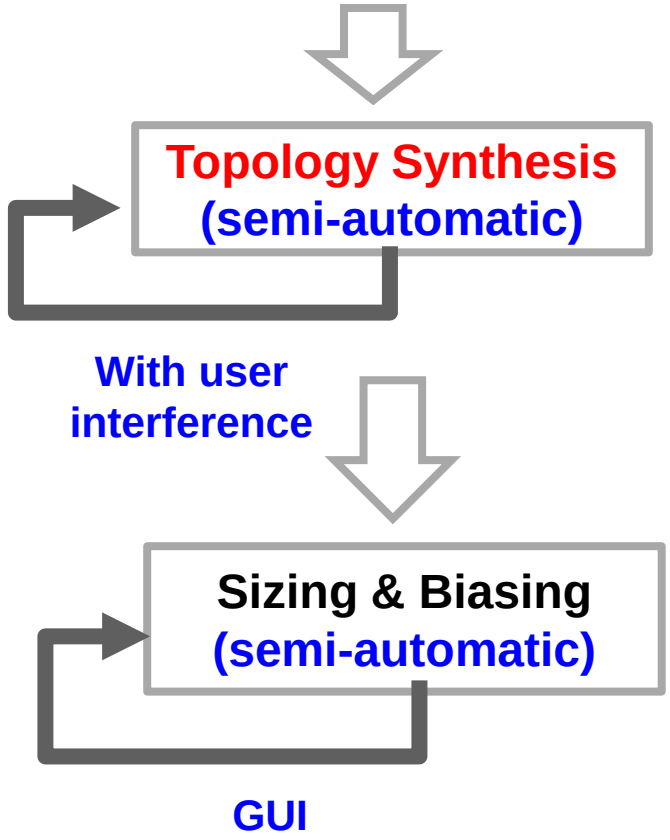
- **Process and external I/Os**
  - **Temperature, external load,**
  - **voltage supply, I/O protection,**
  - **process variations, packaging, etc.**

Scenario for Analog Automation

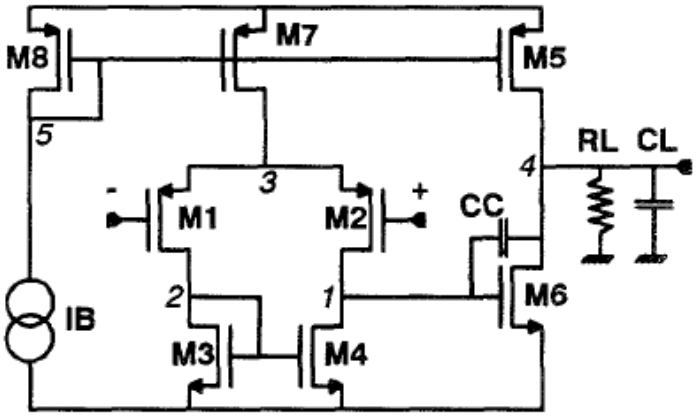
Full automation flow

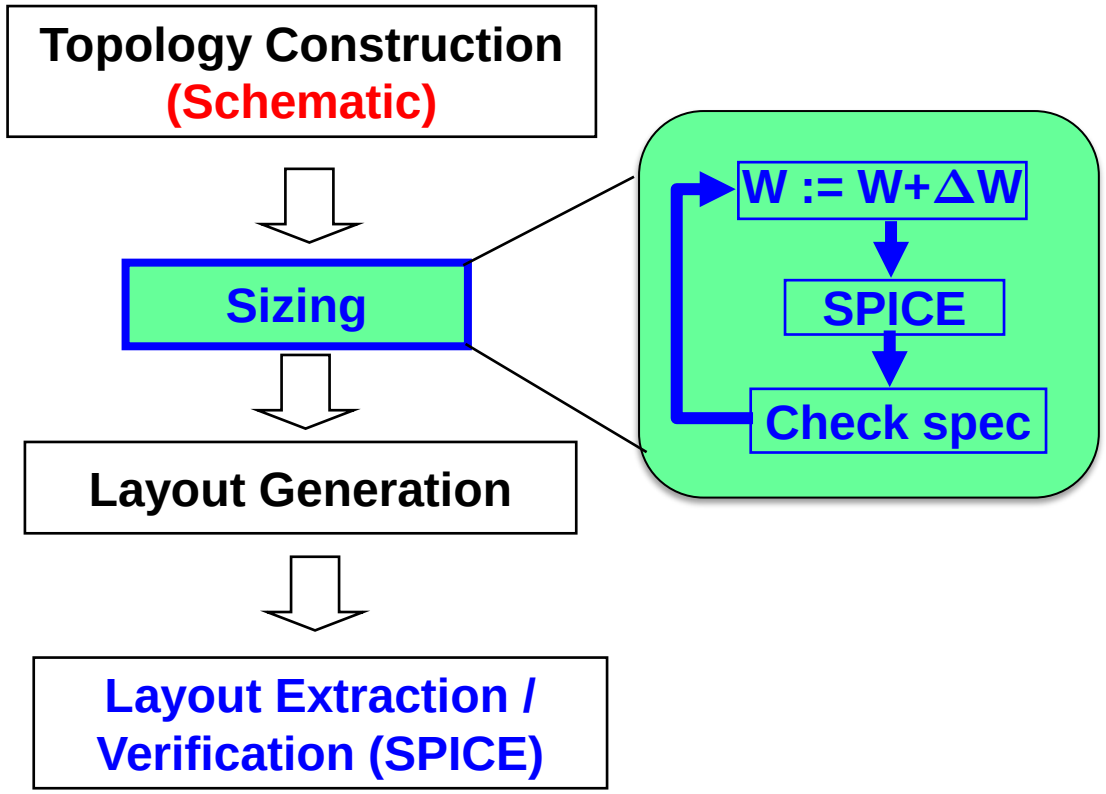


Semi-automation flow



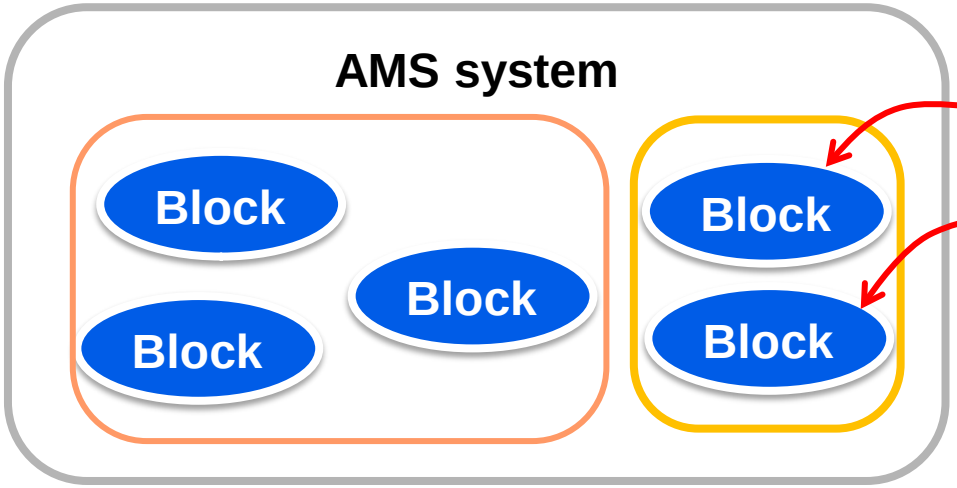
Even “auto-sizing” is nontrivial





System-level Mixed-Signal Design

System-Level Design



Design the blocks in parametric IP (P-Cells) ➔
Better opportunity for system-level optimization & design automation

Nowadays AMS can be described by design languages (Verilog-AMS)

But mapping to circuit implementation is not fully automatic yet (refer to Cadence design tools).

System-Level Verification

- **Commercial tools supporting Verilog/VHDL-AMS can be used for verifying components & systems**
- **but have limitations:**
  - **Lack of application specific libraries;**
  - **Demanding skills to develop cell library.**

- **MATLAB/Simulink is still commonly used as system-level simulator**
  - **But less helpful when moving toward circuit implementation**

Trends – toward digitally assisted AD

- **Digitally assisted analog design is now in the mainstream**
  - **That makes analog design more mixed-signal**
  - **Signal sensing and feedback highly critical**
  - **Requiring good expertise in system design**

- **Texas Instruments (TI) has shifted (around 2004) to controlling and calibrating analog circuits with a dedicated ARM processor**
- **e.g., using a proprietary 64-bit RISC core to actively adjust the linearity of RF circuits.**

- **TI also developed on-chip, low-drop-out (LDO) regulators for precision voltage supply,**
- **and even using an LDO-per-block architecture for critical RF and mixed-signal functions.**

Trends – Combining Digital with Analog

- **Main philosophy – Combining digital control with analog design !**
- **Theresa Meng (Stanford University professor) edaboard.com, 2004**
- **“We are using logic circuits to calibrate and correct analog circuits. ”**
- **“But with digital circuitry being so much smaller and using one twentieth the power, tomorrow we will be asking ourselves just how many analog transistors we need to keep at all.”**
- **"We have to challenge traditional design. ”**
- **“We can do self-calibrating circuits that continuously correct distortion.”**
- **“This takes new topologies and new digital algorithms for statistical signal processing. But it is the future of analog."**

Simulation Tools

Recommended

- **HSPICE**
- **Cadence tools (Spectre, etc)**
- **PSpice (www.orcad.org)**
- **LTspice (www.linear.com)**
  - **A simulator by Linear Technology Corp**
  - **PC version available**
  - **With mixed-signal functionality**
  - **Recommended for use in this class!**

Webpage for Courseware Download

- **For courseware download and assignment submission:**

- **http://202.120.46.7/html/courseware.htm**
  - **(maintained by the MSDA Lab)**
- **http://edalab.sjtu.edu.cn/login/index.php (disabled)**

- “混合信号电路设计与自动化方法（硕）”

References

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