Lecture 3. Opamp Design Basics

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- Opamp specs
- Building blocks
- Circuit-level design of LM741
- Terminologies
  - Input Common Mode Range (ICMR)
  - Offset voltage/current,
  - Output impedance, slew rate, noise
  - PMRR, CMRR,
  - Gain/phase margin, etc.
- Simple design tips

Opamp Design Basics

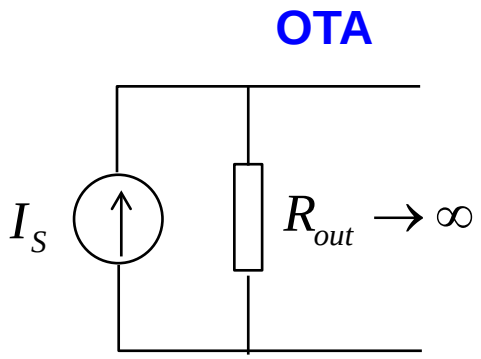
Opamp Design Metrics

- **Design parameters**
  - **Input bias current**
  - **Input offset voltage**
  - **Input offset current**
  - **Output impedance**
  - **Slew rate (SR)**
  - **Noise**
  - **Distortion**
  - **CMRR**
  - **PSRR**
  - **Gain and phase margins**
  - **Power & speed**

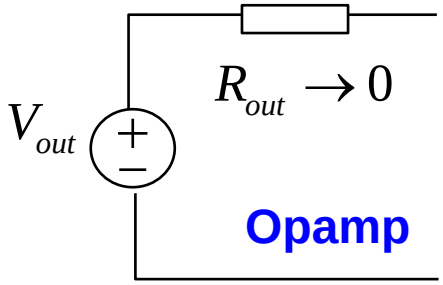
- **It's not possible to achieve all these goals by one single opamp stage.**
- **That's way we need to learn multi-stage opamp design.**

Opamp Basics

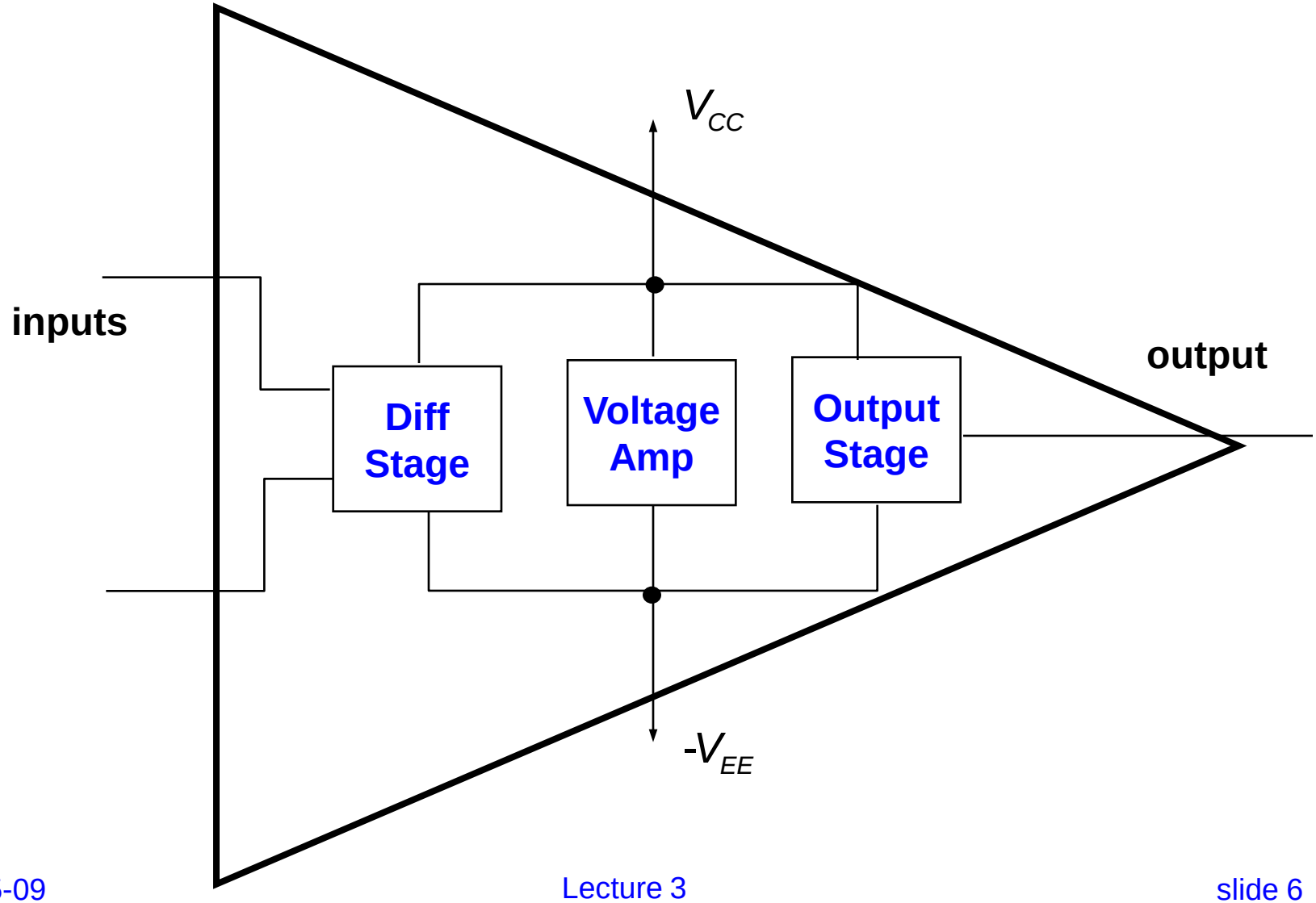
- **Opamp basics**
  - **Biasing circuit**
  - **Differential input stage**
  - **Voltage gain stage**
  - **Output stage**



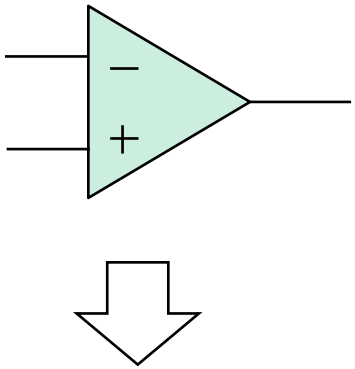
- **Feature of opamps**
  - **Very high input impedance (drawing no current)**
  - **Very low output impedance (as voltage source)**
  - **Very high open-loop gain**
  - **Differential input stage**
  - **Feedback for stability**



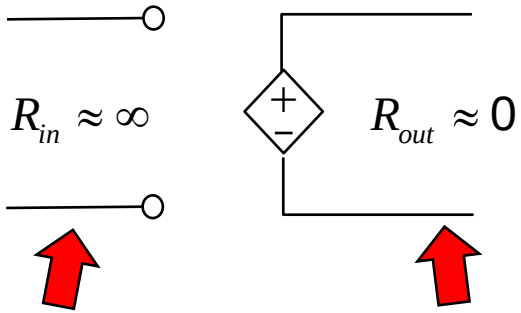
Typical Opamp Building Blocks



Opamp as a VCVS

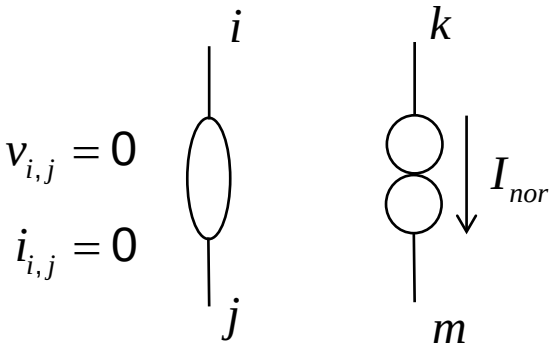


VCVS model



High input impedance

Ideally zero output impedance



Nullator **Norator**

$$v_{k,m} = arbitrary$$

$$i_{k,m} = arbitrary$$

Ideally it can be modeled by a nullor (a pair of nullator & norator)

Opamp Applications

- **Opamp has many applications**
  - **Comparators (infinite gain, open-loop)**
  - **Oscillators (open-loop opamp)**
  - **Filters (Switched-capacitor circuits)**
  - **Sensors**
  - **Sample and Hold (S&H)**
  - **Instrumentation amplifier**
  - **DC-DC converter**

What is Biasing ?

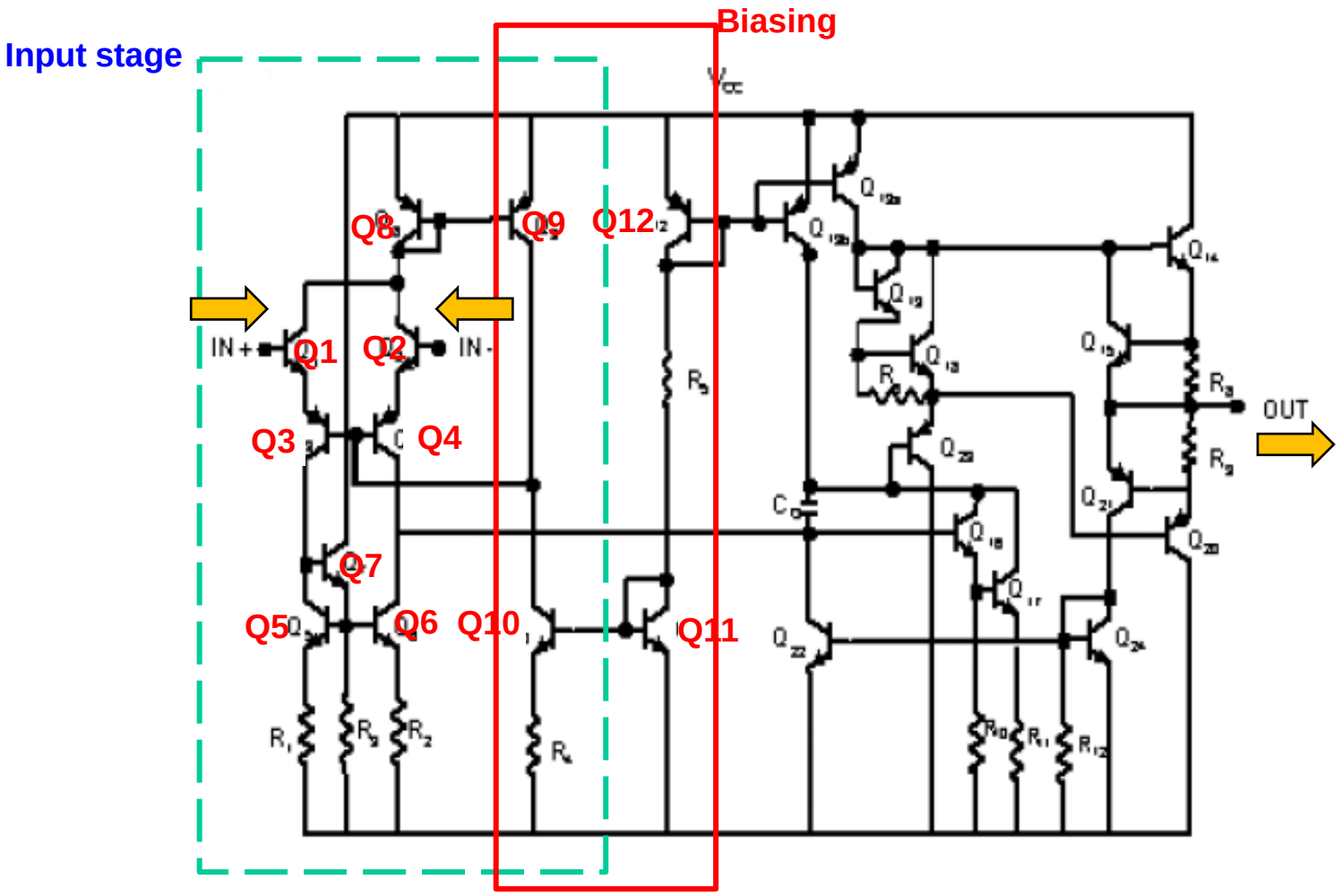
- **Transistor Biasing is the process of setting a transistor's DC operating voltage/current conditions properly so that any AC input signal can be amplified efficiently.**

- **If a transistor is properly biased to have a suitable operating point (OP), it can operate like a linear amplifier nearby the OP.**

Opamp Structure

Using bipolar LM741 as an example

Opamp LM741 Circuit

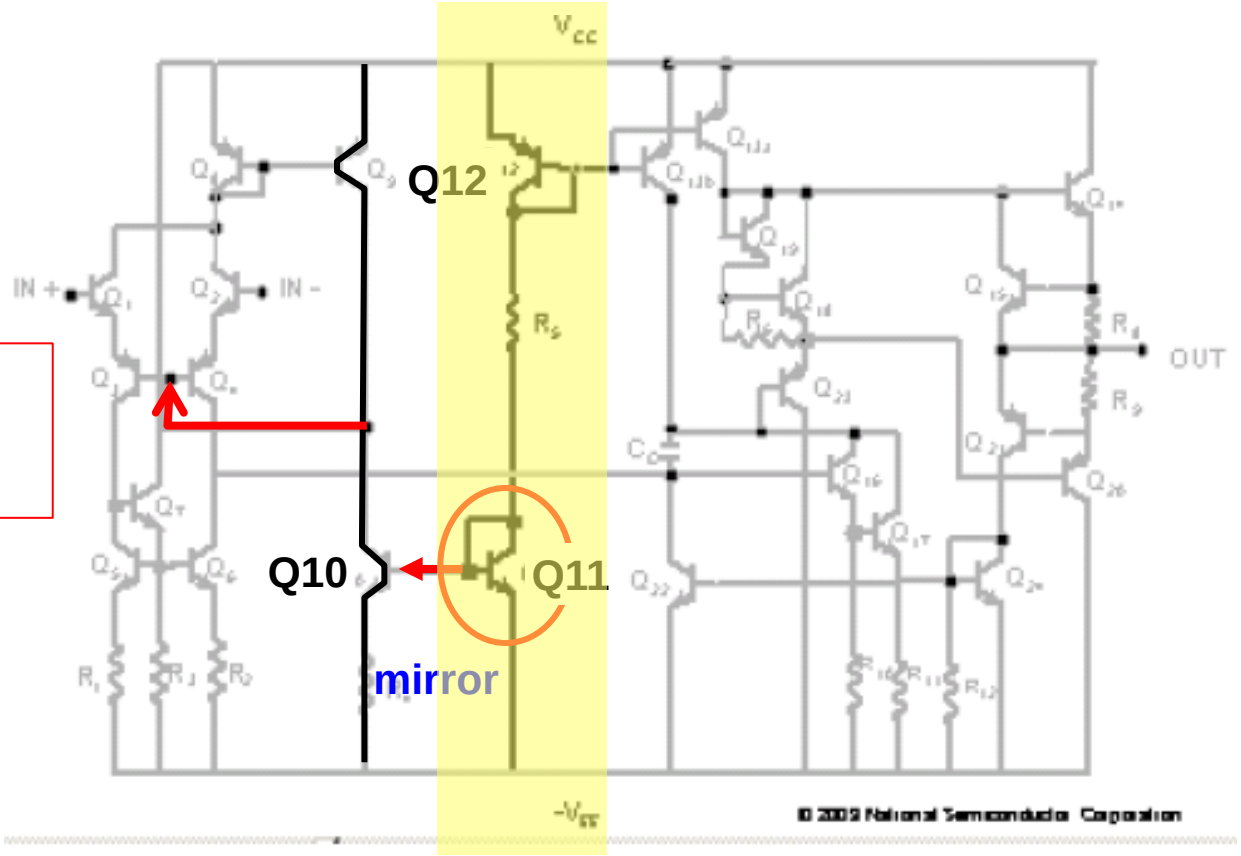


Biasing Circuit

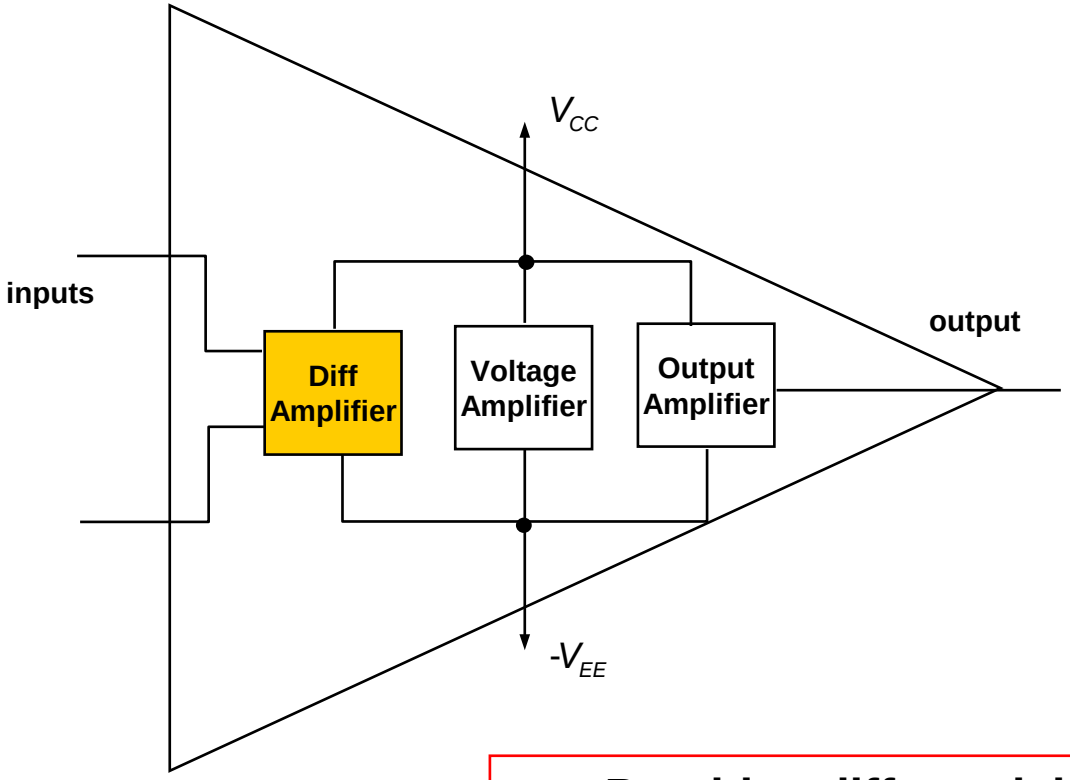
The branch of "Q12, R5, Q11" provides the biasing current.

The current is delivered to the input stage by the mirror pair (Q10, Q11).

providing bias current to input stage

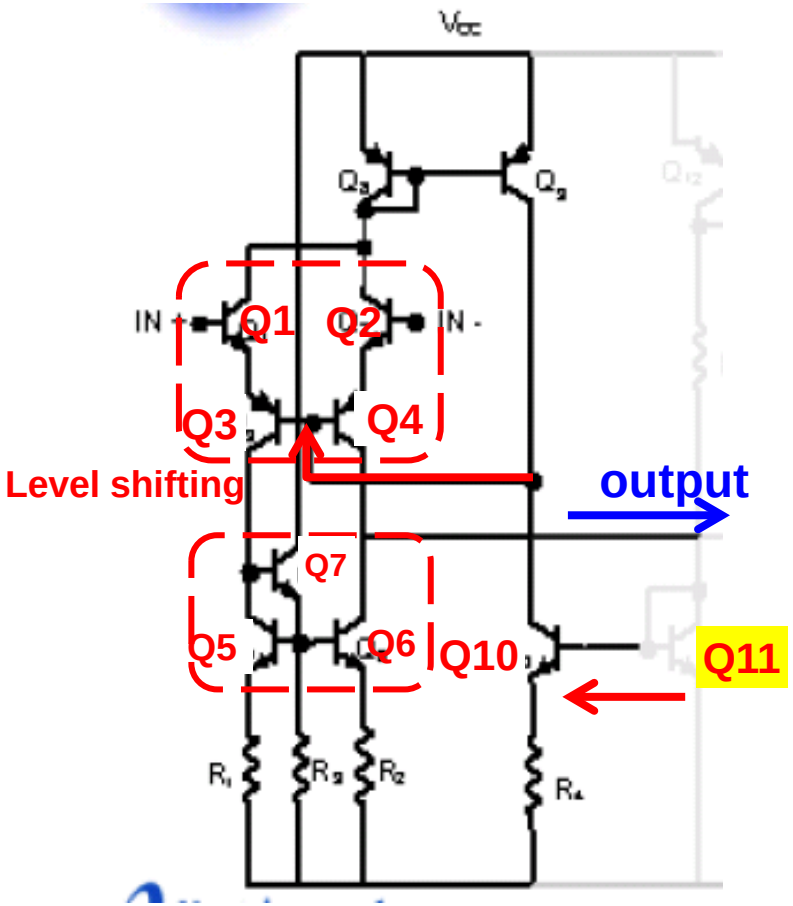


Differential Amplifier (Input)



- Provides differential input and dc gain
- With high input impedance
- Drawing negligible input current

Differential Input Stage

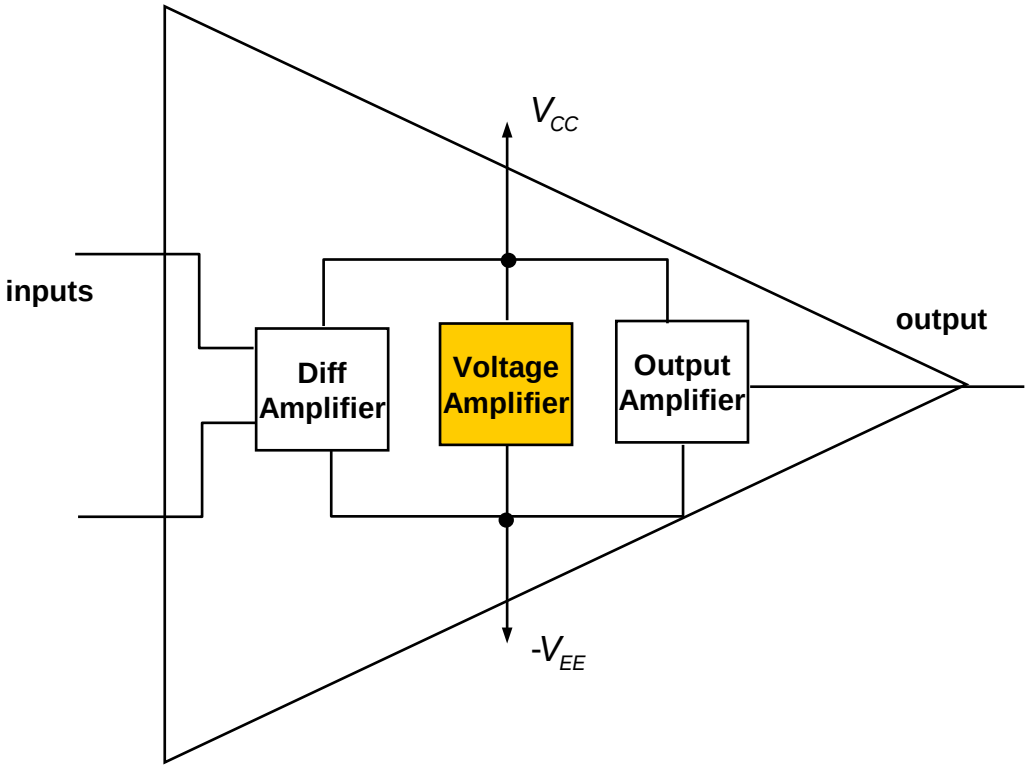


(Q1, Q2) connected with (Q3, Q4) as emitter followers – giving high input impedance.

(Q3, Q4) provide dc level shifting.

(Q5, Q6, Q7) load the input stage and converts differential signal to single-ended signal

High-Gain Voltage Amplifier (Middle)



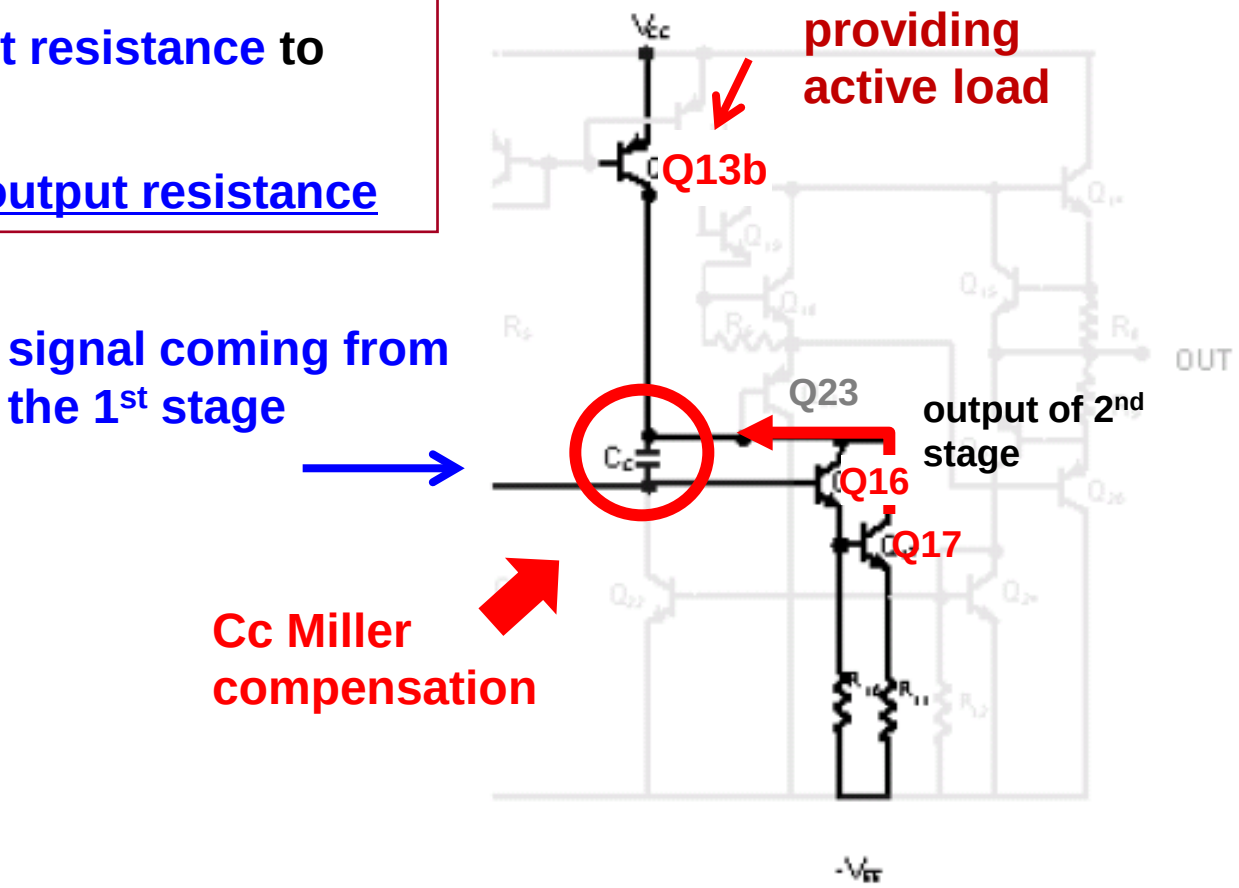
- **Provides voltage “gain”**
- **Conveying it to the output stage**

Voltage Gain Stage (Middle)

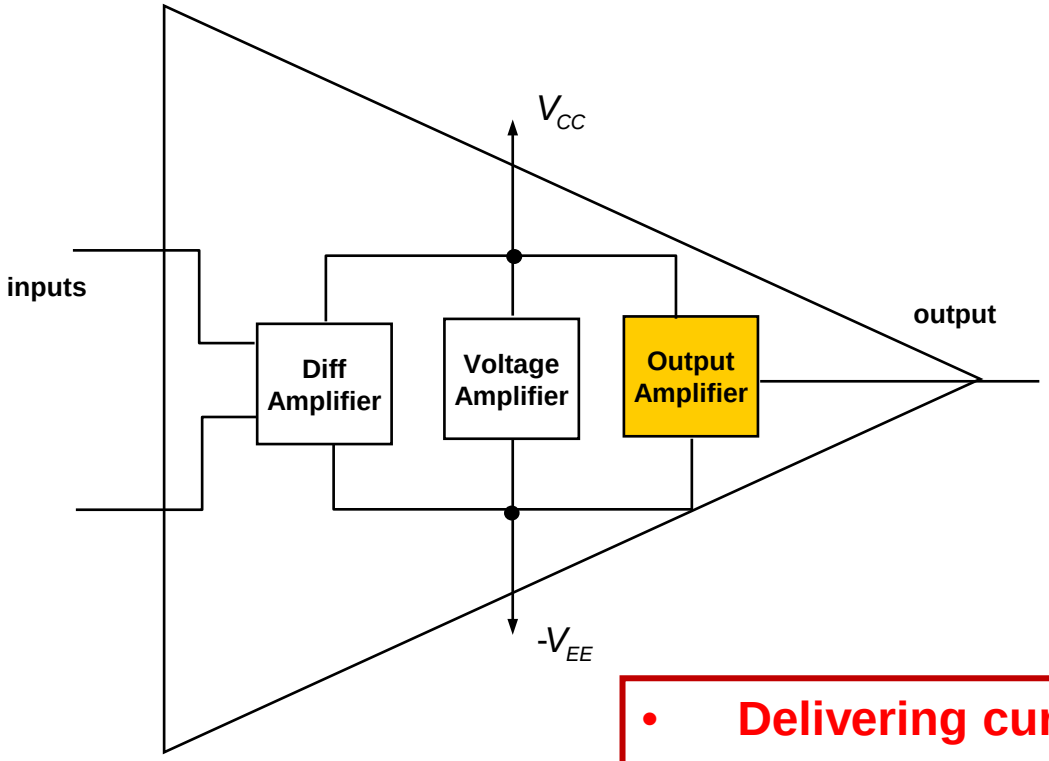
Q16-Q17 emitter follower

giving **high input resistance** to this stage;

Providing **high output resistance**



Low Impedance Output Stage



- **Delivering current to the load;**
- **Very low output impedance (minimize self-loading)**
- **Providing short circuit protection**

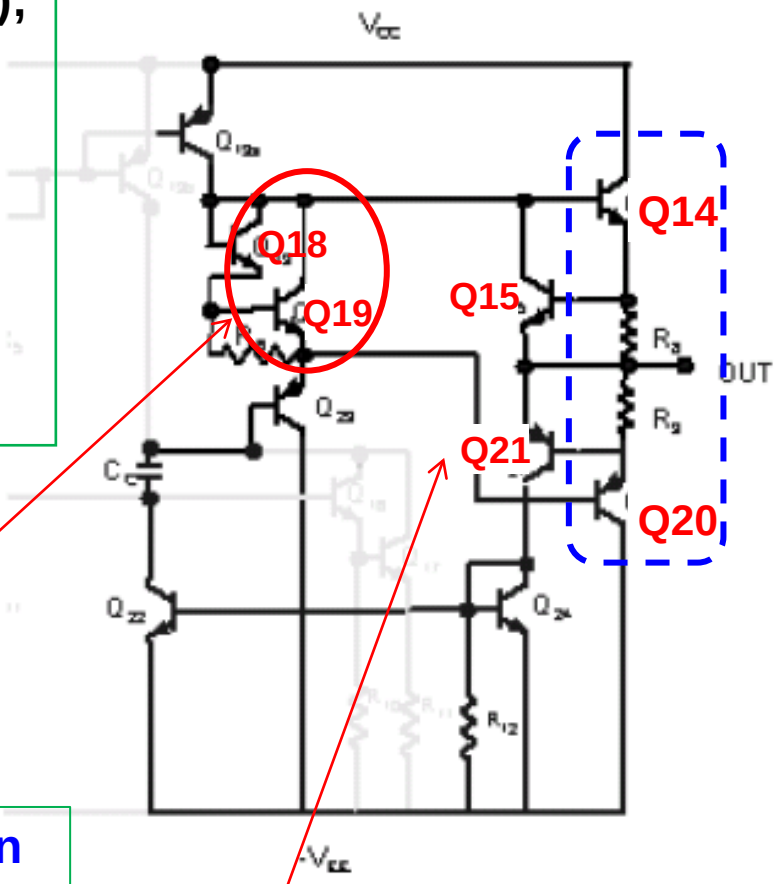
Class AB Output Stage

(Q14, Q20) form complementary output stage (class AB, better power efficiency);

supplying fairly large (positive/negative) current to load;

Negligible temperature effect.

Low output impedance.



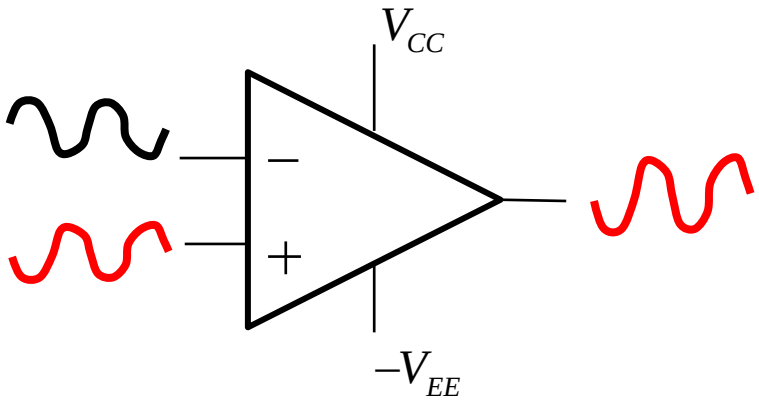
(Q18, Q19) bias the output transistor in linear region

(Q15, Q21) for short circuit protection by shunting overflow current

Summary

- **CMOS opamp circuit can be analyzed analogously**
- **Stage-based design helps intuition**
- **An opamp has a main signal path and some feedback compensations**
- **Detailed analysis has to go small-signal**

Differential Input



Input signals are 180 degree out of phase.

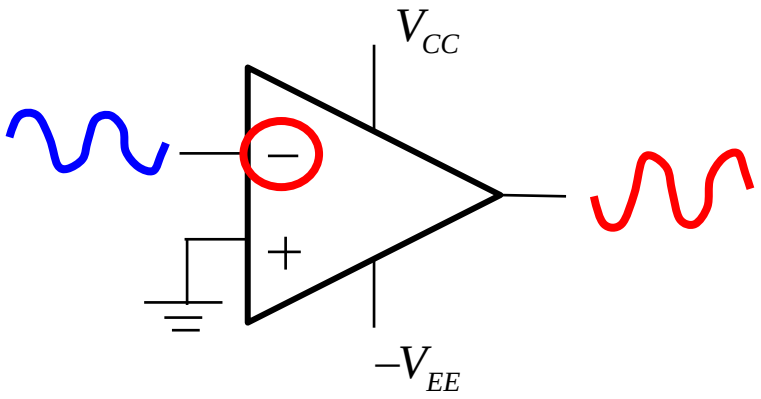
Output is in-phase with the non-inverting input.

In general, op-amps can be set up in three different input modes:

- **(1) differential input mode,**
- **(2) inverting input mode,**
- **(3) non-inverting input mode.**

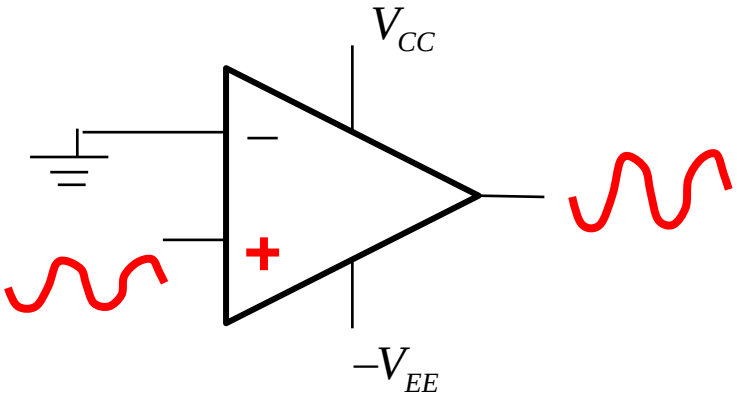
When the input signals are in-phase, there should be no output. Such input signal is called the common-mode signal (this property is used in testing opamp)

Opamp working @ Inverting Input Mode



- **The non-inverting input is grounded or connected to a fixed supply.**
- **The output is 180 degree out of phase with the input.**

Working @ Non-inverting Input Mode



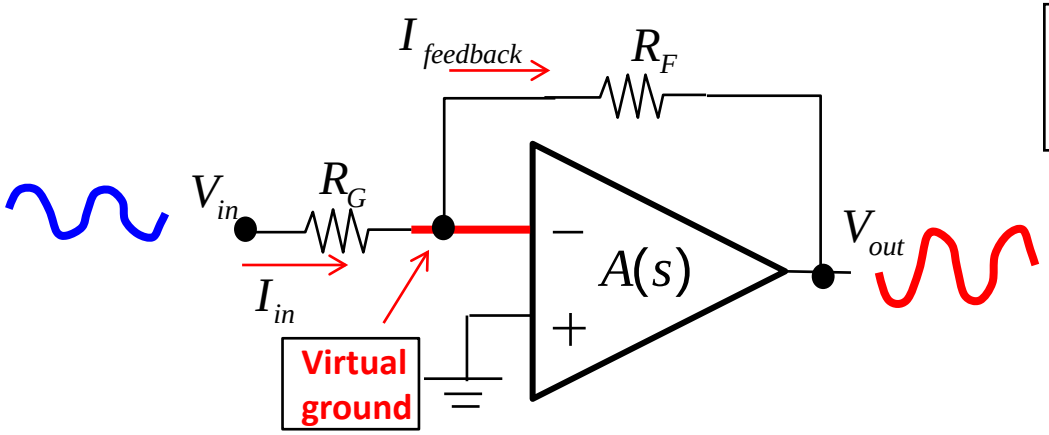
- **The inverting input is grounded.**
- **The output is in-phase with the input.**

Open-loop vs Closed-loop

- **Open-loop**
  - **Very high gain**
  - **Noise and other "unwanted" signals are amplified by the same gain factor (poor stability)**
  - **Open-loop used in comparators and oscillators (intentionally making use of instability)**

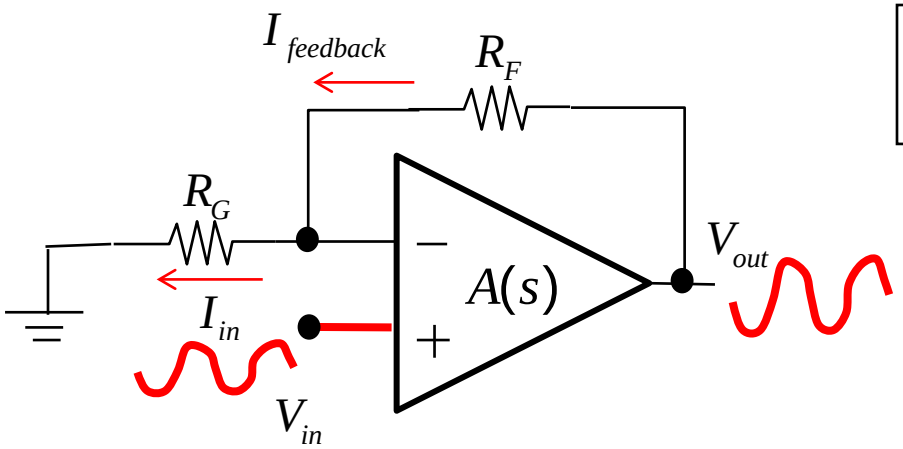
- **Closed-loop**
  - **Reduces the gain of amplifier**
  - **But improves the stability**
  - **Most applications use closed-loop opamps**

Closed-Loop Configurations



Inverting closed-loop (out of phase)

$$\frac{V_{out}}{V_{in}} = -\frac{R_F}{R_G}$$



Non-Inverting closed-loop (in-phase)

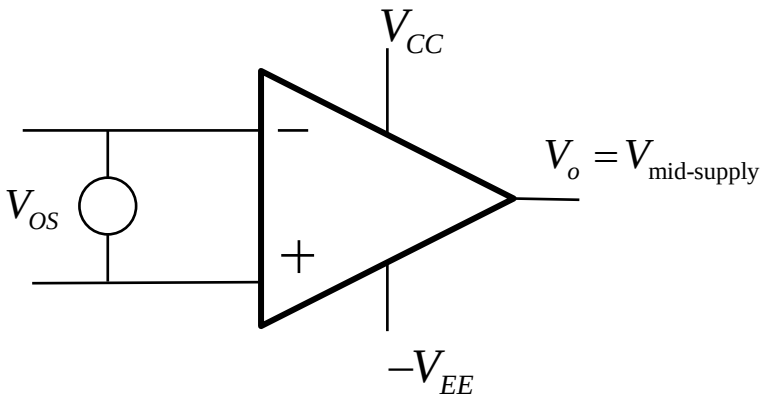
$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_F}{R_G}$$

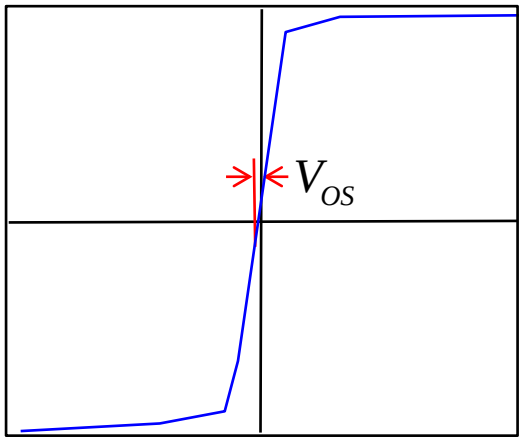
Detailed Definitions of Opamp Metrics

- **Input offset voltage, Input bias current, Input offset current**
- **Output impedance**
- **Internal/external noise**
- **CMRR / PSRR**

Input Offset Voltage

- **Ideally, when the two inputs are equal ($\Delta = 0$), the output should be at the mid-supply.**
- **In reality (due to dc offset of the circuit) we have to apply a small input dc voltage difference to make the output settle at the mid-supply.**
- **Such a dc input voltage difference is called the "Input Offset Voltage (V_{OS})".**



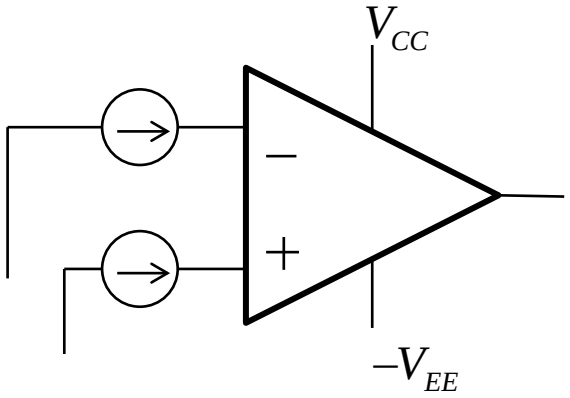


Input Bias Current

- **Ideally should be zero, but practically not.**

- **Positive input bias current:**
  - **Small current seen on the non-inverting input**
- **Negative input bias current:**
  - **Small current seen on the inverting input**

- **Input bias current (I_{BIAS})**
  - **Average of the two currents at the inputs.**

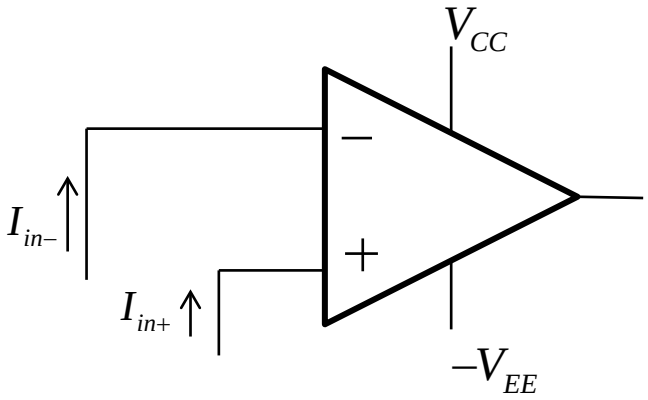


Input Offset Current

- **Ideally input currents should be equal to obtain zero output voltage.**
- **In reality, one has to set unequal input currents to make the output voltage zero.**

- **Input offset current (I_{OS}): is the difference of the two input currents to achieve the zero output voltage.**

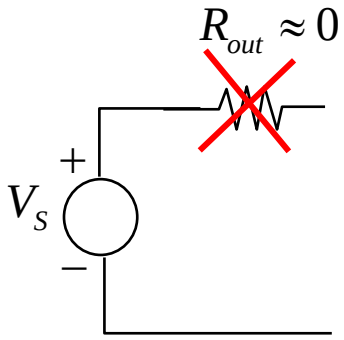
$$I_{OS} = I_{in+} - I_{in-}$$



Output Impedance (Z_{OUT})

- **Ideally should be zero.**

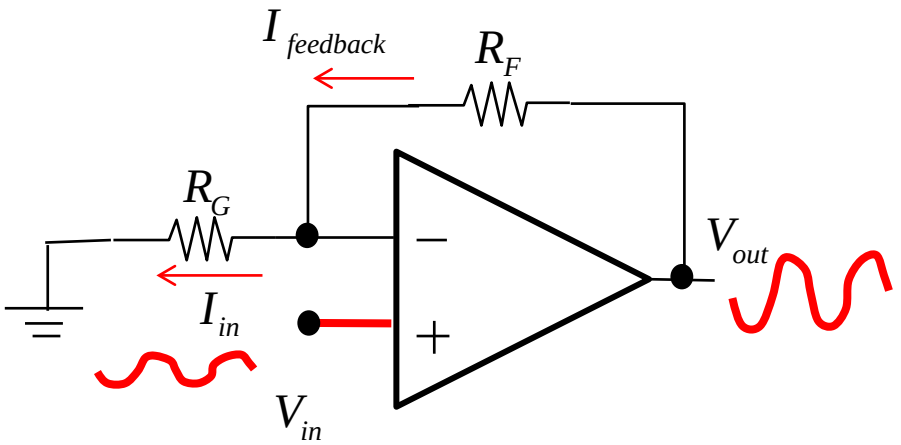
- **It is usually "assumed" to be zero**
  - **This way an op-amp behaves like an ideal voltage source.**
  - **It is capable of driving a wide range of loads.**



Internal Noise

- **Caused by internal components, bias current, and drift.**
- **Internal noise can be converted to "input referred noise".**
- **Noise or "unwanted" signal is amplified along with the "wanted" signal.**
- **Noise is amplified from the non-inverting input with a noise gain:**
- **Noise gain = 1 + (R_F/F_G)**

$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_F}{R_G}$$



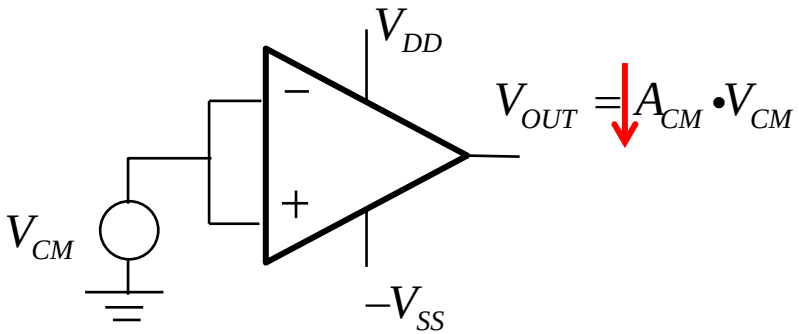
External Noise

- **Caused by external electrical devices and components**
  - **Power supply noise**
  - **Feedback resistor noise**
  - **Package noise**

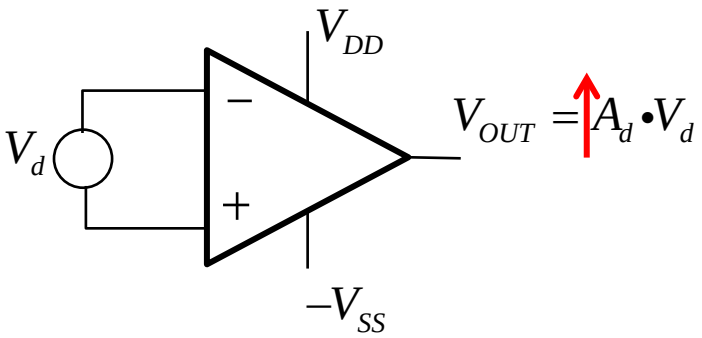
- **These noises can be suppressed by proper circuit construction technique**
  - **Adequate shielding**
  - **Reduce resistor values when possible**

Common Mode Rejection

- **When both inputs have the "common" voltage, such a signal is called a common mode signal.**
- **Output should be ideally zero for the common mode input, i.e., common-mode rejection.**
- **A basic feature of differential amplifiers**



Common mode gain (A_{CM})



Differential gain (A_d)

CMRR

- **Common Mode Rejection Ratio (CMRR)**
- **Ratio of differential gain (A_d) to common-mode gain (A_{CM}), expressed in dB.**
- **Typically decreases with frequency.**

$$CMRR = 20\log\left|\frac{A_d}{A_{CM}}\right| = 20\log\left|\frac{\Delta V_{OS}}{\Delta V_{CM}}\right|$$

A_d : Differential gain

A_{CM} : Common mode gain

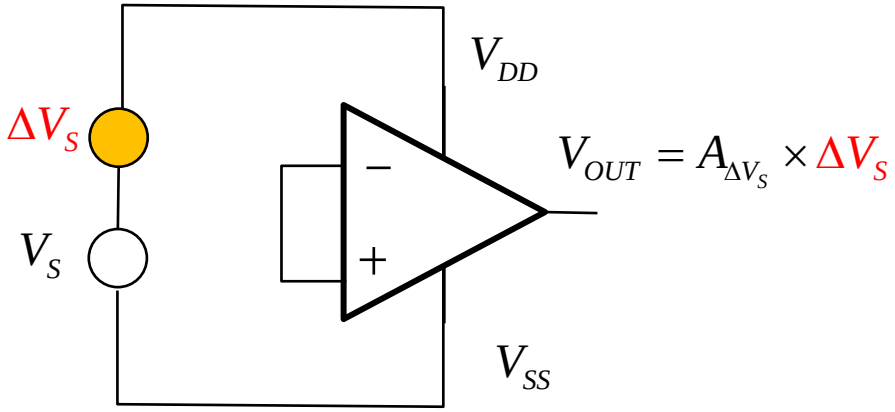
V_{OS} : Offset voltage (output)

V_{CM} : Common mode voltage (output)

There is another simulation-based measurement method for CMRR (see another lecture)

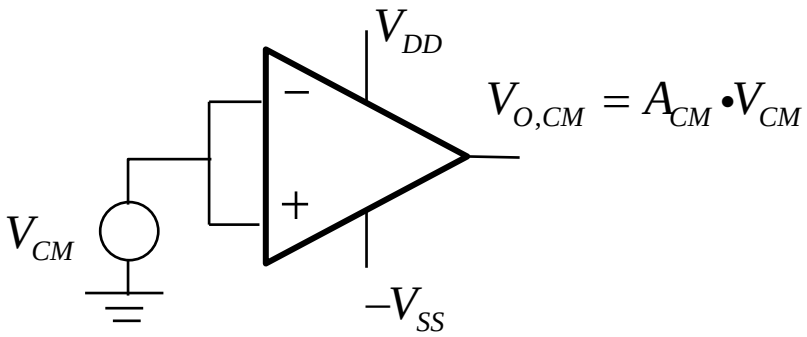
Power Supply Rejection Ratio (PSRR)

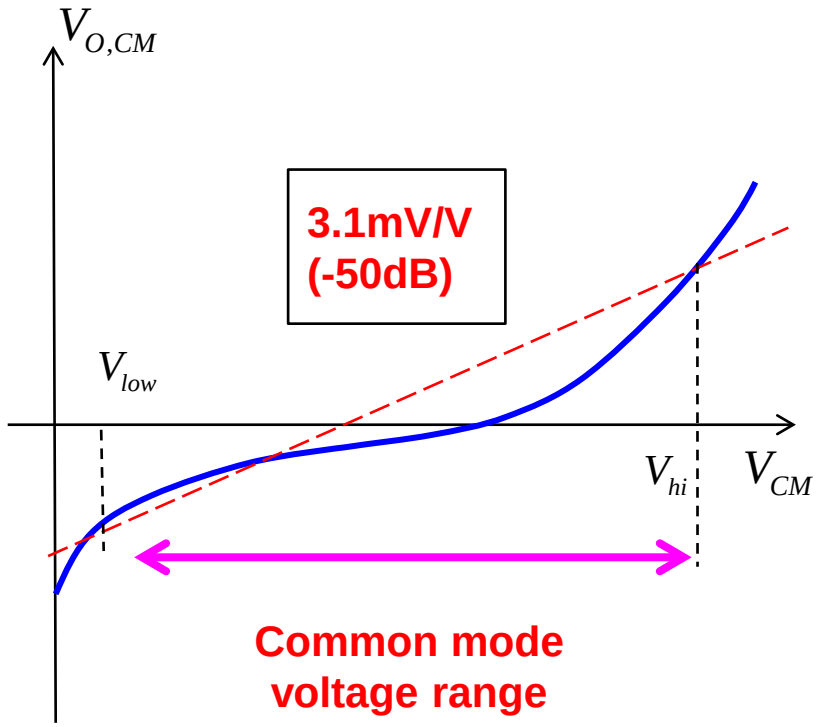
- **Ratio of differential gain to small-signal gain of the power supply**
- **Or ratio of change in offset error to change in power supply voltage**



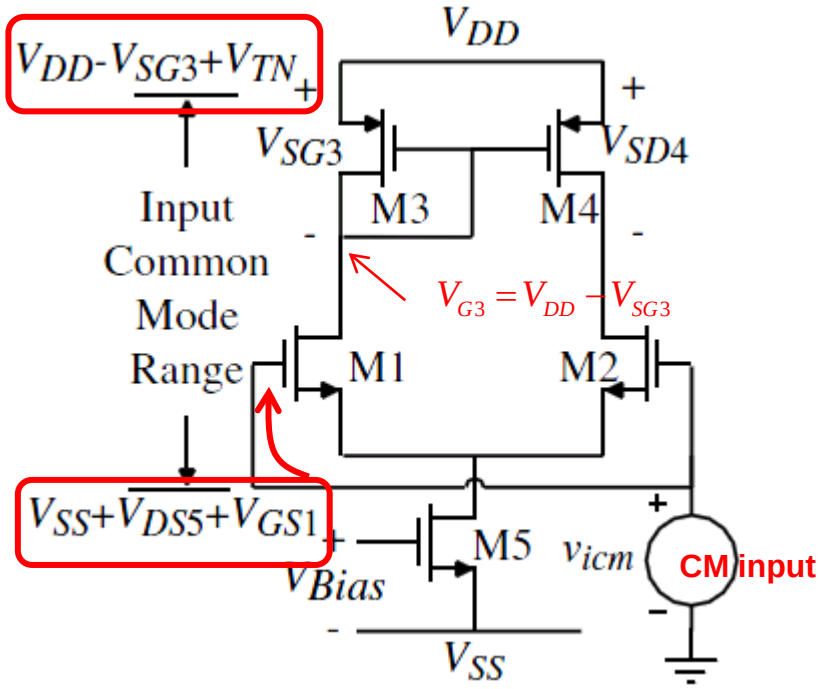
Common Mode Voltage Range

Range of the common input voltage V_{CM}, [V_{low}, V_{hi}], within which the differential pair behaves as a linear amplifier.





Input Common Mode Range



Diff amp. with a current mirror load

ICM Range is the largest voltage interval that the CM input can swing.

Max of $V_{cm,in}$:

$$V_{DD} - V_{SG3} + V_{TN}$$

(V_{G3})

Min of $V_{cm,in}$:

$$V_{SS} + V_{DS5} + V_{GS1}$$

$$V_{DS1} \geq V_{GS1} - V_{TN} \quad \Rightarrow \quad V_{G1,\max} = V_{D1} + V_{TN}$$

$$= V_{G3} + V_{TN}$$

Courtesy Paul Allen's lecture

Input Common Mode Range

higher

$$V_{SD3} = V_{SG3} - |V_{TP}| \le V_{SG3}$$

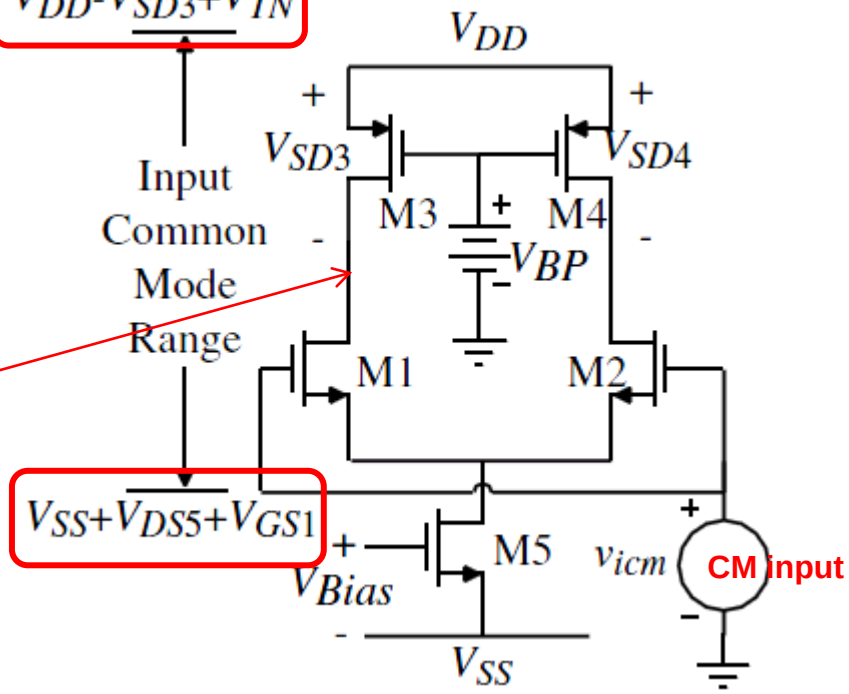
V_{DD}-V_{SD3}+V_{TN}

$$\Rightarrow \quad V_{DD} - V_{SG3} + V_{TN} \le V_{DD} - V_{SD3} + V_{TN}$$

Input Common Mode Range

$$V_{D1} = V_{G3} = V_{DD} - V_{SD3}$$

V_{SS}+V_{DS5}+V_{GS1}



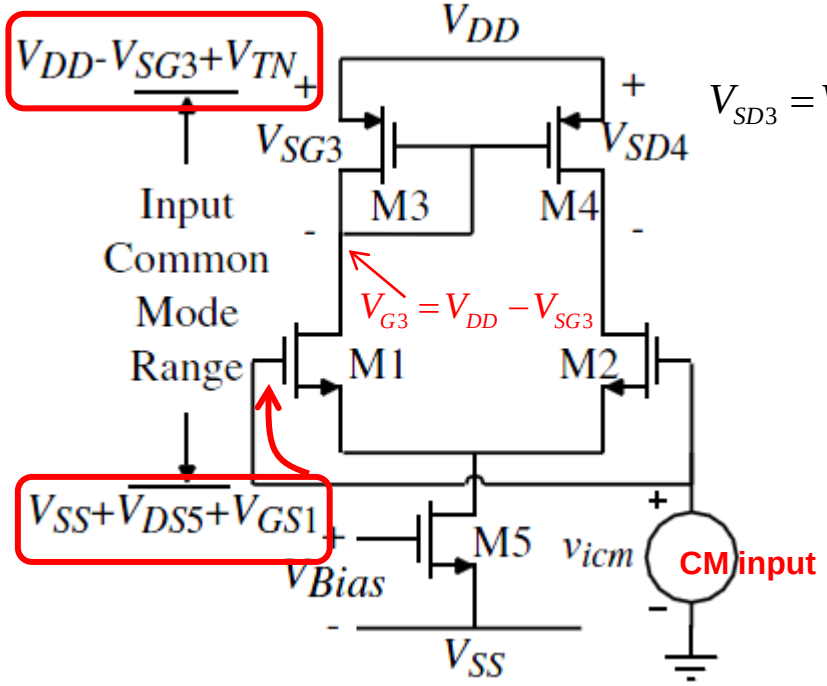
Diff amp. with a current source load

$$V_{DS1} \ge V_{GS1} - V_{TN} \quad \Rightarrow \quad V_{G1,\max} = V_{D1} + V_{TN} = V_{G3} + V_{TN}$$

Using current source load improves the ICMR.

Courtesy Paul Allen's lecture

ICM Range (Comparison)



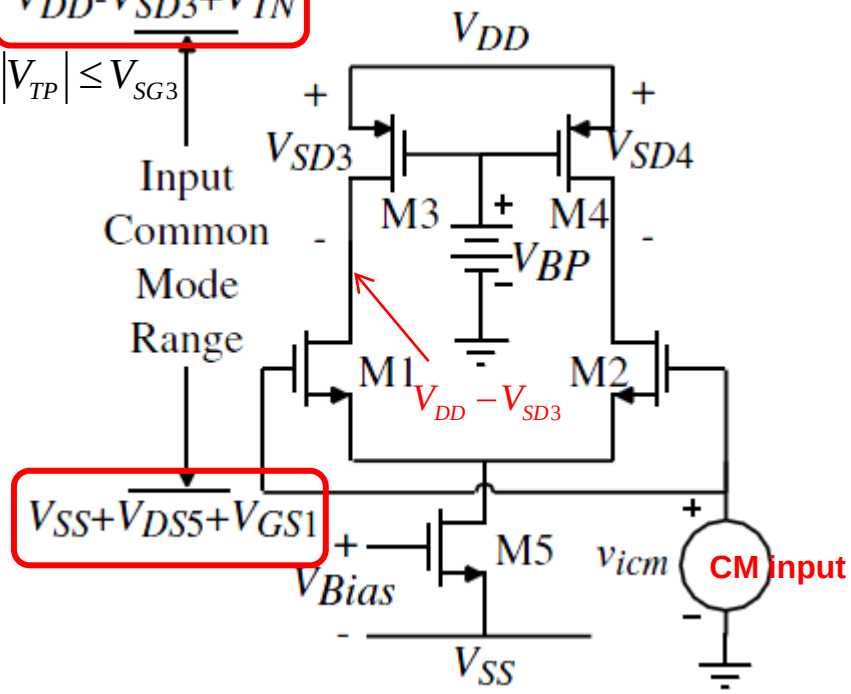
Diff amp. with a current mirror load

higher

V_{DD}-V_{SD3}+V_{TN}

$V_{SD3} = V_{SG3} - |V_{TP}| \leq V_{SG3}$

$V_{G1,\max} = V_{D3} + V_{TN}$



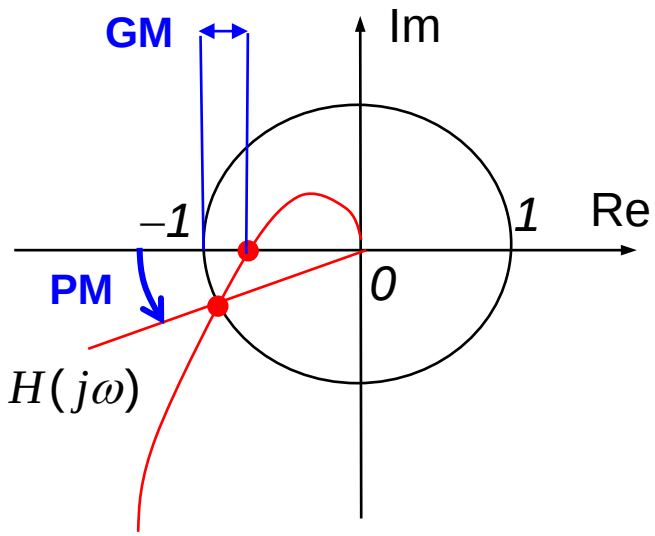
Diff amp. with a current source load

Using current source load has better ICMR.

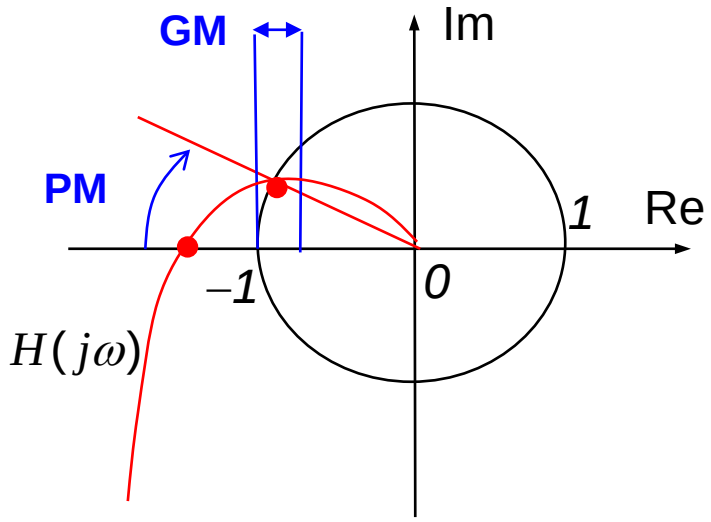
Courtesy Paul Allen's lecture

Gain and Phase Margins

- **Gain Margin (GM)**
  - **Gain of the amplifier at the point where the phase is 180°.**
  - **If this gain is larger than unity, the amplifier in closed-loop is unstable.**

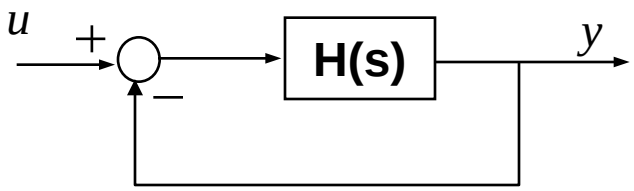


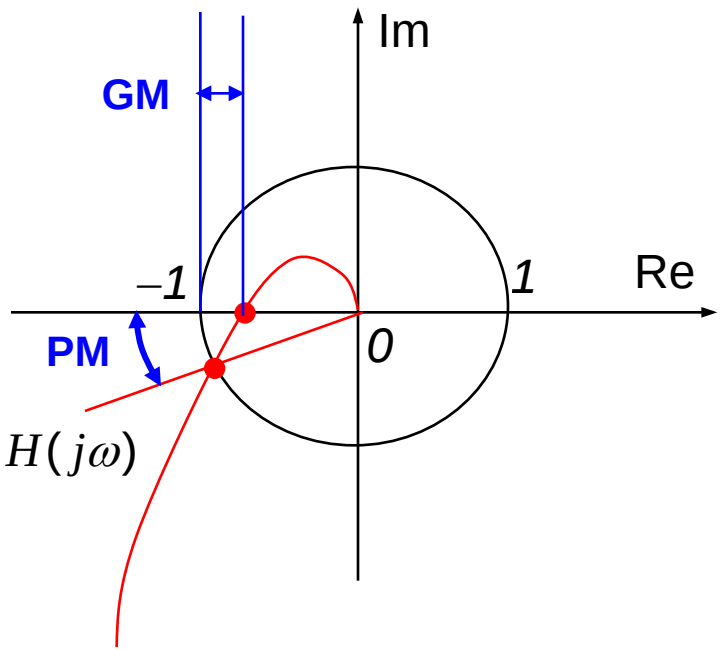
- **Phase Margin (PM)**
  - **Difference between the phase at the unity gain (0dB) and 180°.**
  - **If the phase lag is greater than 180°, the amplifier in closed-loop is unstable.**

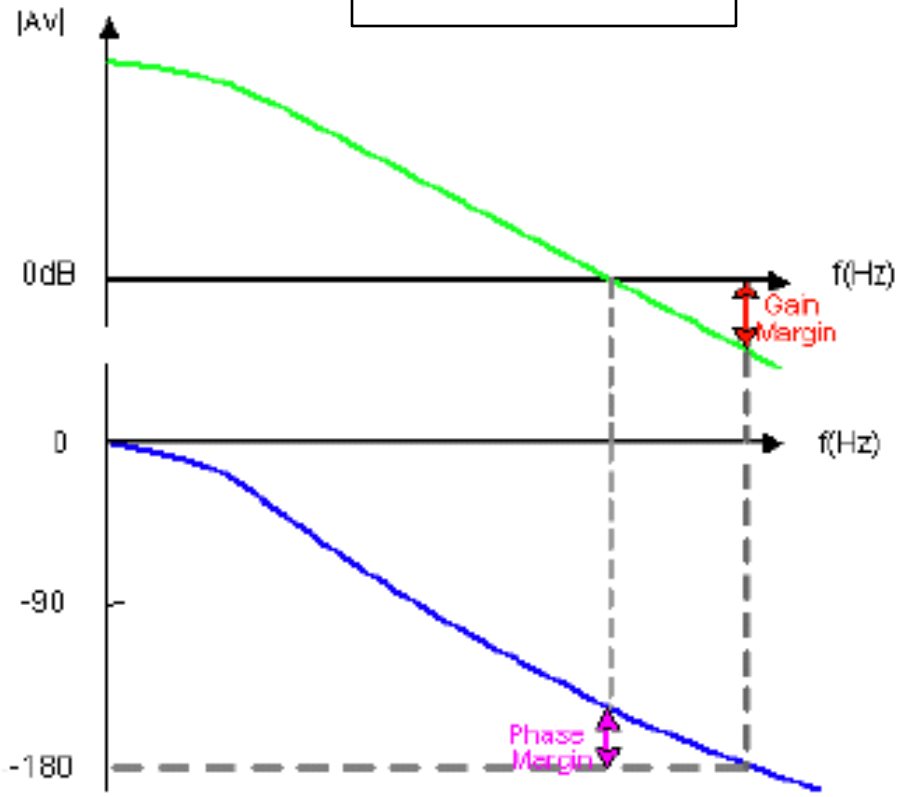


Gain and Phase Margins

$$\frac{Y(s)}{U(s)} = \frac{H(s)}{1 + H(s)}$$





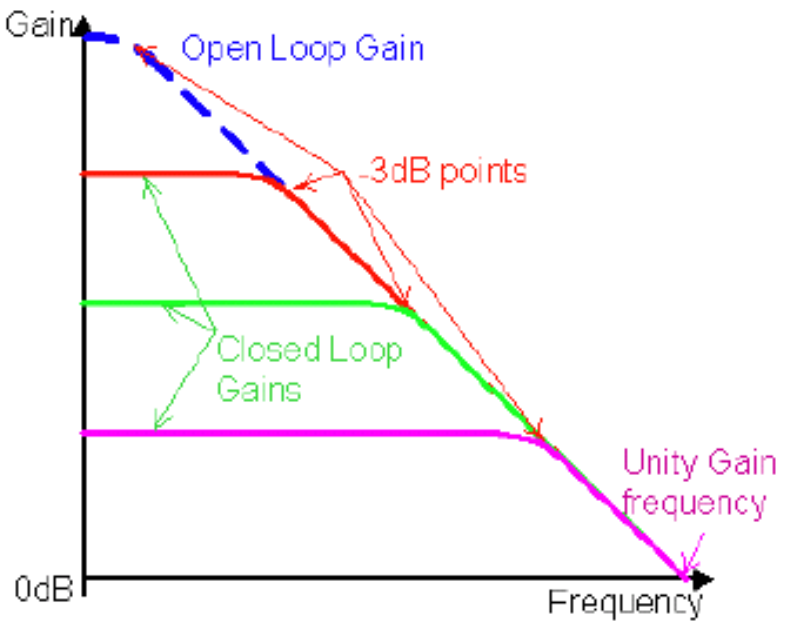


Bandwidth (BW)

BW is measured at the point where gain falls by 3dB (0.707 = 1/sqrt(2) of the max gain.)

Open-loop operation has extremely low BW.

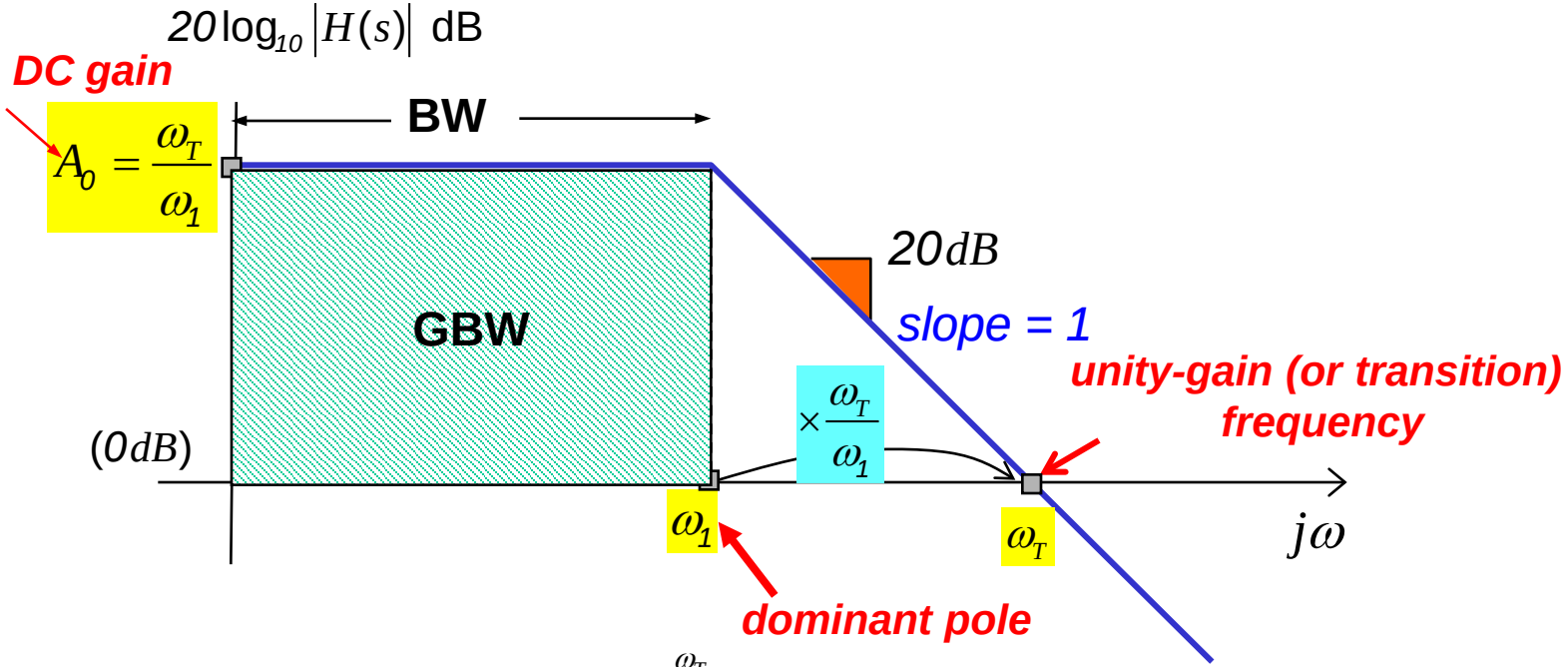
Closed-loop significantly increases BW (but reduces the low-freq gain).



Gain * Bandwidth = GBW = Unity Gain Frequency

GBW is fixed hence specified in datasheet while gain (depending on feedback) is set by the user.

Freq-domain Metrics



$$H(s) \approx \frac{\omega_T}{s+\omega_1} = \frac{\frac{\omega_T}{\omega_1}}{1+\frac{s}{\omega_1}}$$

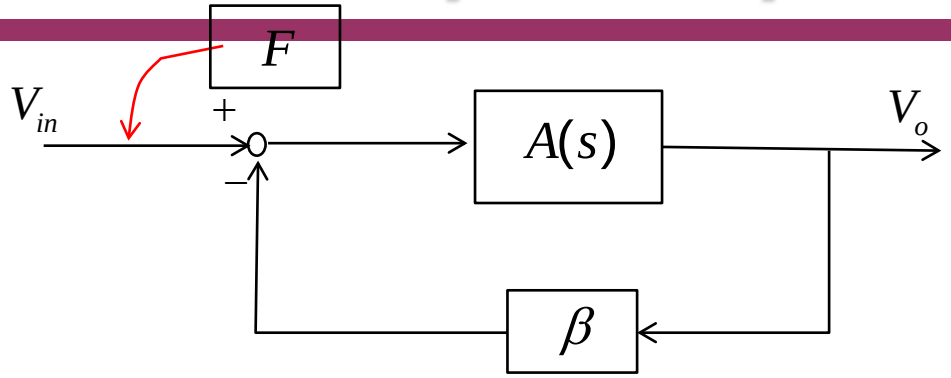
$$\frac{\omega_T}{\omega_1} \gg 1$$

BW can be estimated by the dominant pole (s = - ω_1) and the DC gain.

GBW = f_T

$$|H(s)|_{s=j\omega_T} = \frac{\frac{\omega_T}{\omega_1}}{\sqrt{1+\left(\frac{\omega_T}{\omega_1}\right)^2}} \approx 1$$

Open-loop, Closed-loop



Open-loop TF: A(s)

$$A(s) \approx \frac{a}{1+\frac{s}{p}}$$

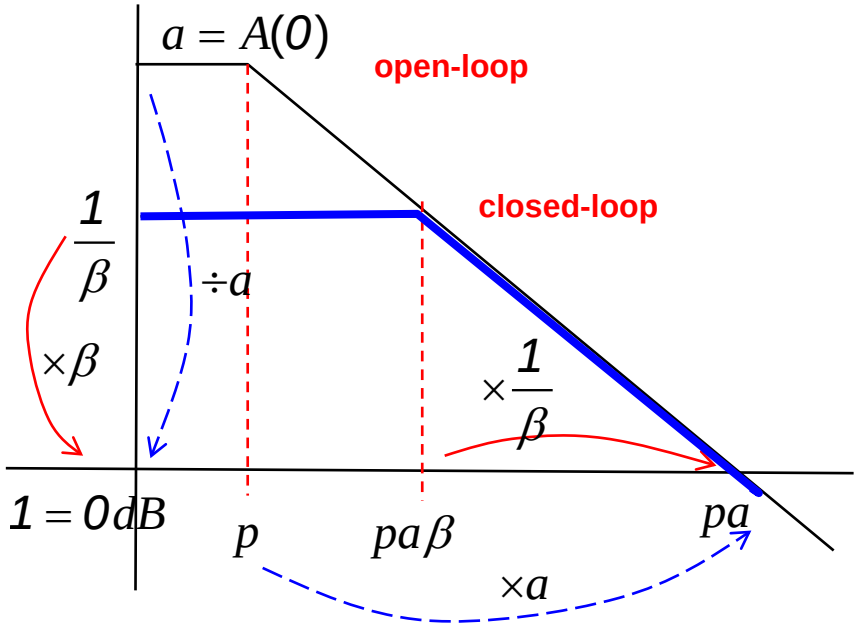
one-pole model

Closed-loop TF:

$$A_{cl}(s) = \frac{V_o}{V_{in}} = \frac{A(s)}{1+\beta A(s)} = \frac{\frac{a}{1+\frac{s}{p}}}{1+\frac{\beta a}{1+\frac{s}{p}}} = \frac{a}{1+\beta a+\frac{s}{p}}$$

$$A_{cl}(0) \approx \frac{1}{\beta} > 1 \qquad \approx \frac{a}{\beta a+\frac{s}{p}}$$

$$\frac{1}{a} < \beta < 1 \quad \Rightarrow \quad \beta a > 1$$

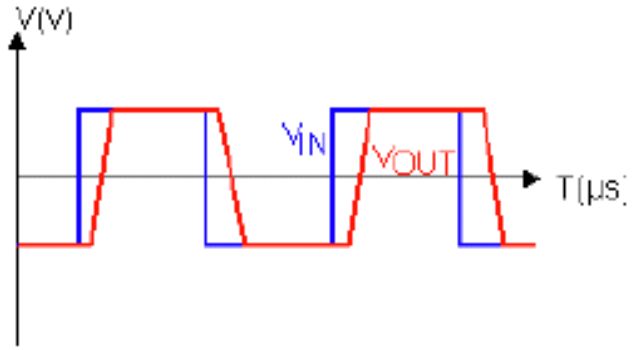


The open-loop dc gain (a) is large

Slew Rate

Maximum rate of the output voltage rising/falling time.

$$SR = \frac{\Delta V_{OUT}}{\Delta t} \quad (V / \mu s)$$



It measures how fast the output signal can "follow" the input signal.

*** We shall discuss in greater details on this subject in a later lecture.**

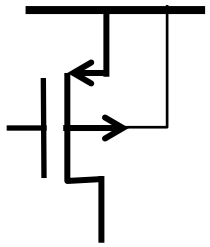
Simple Analog Design Tips

Differential Circuit & Symmetry

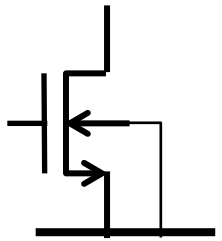
- **Consider to use differential signal path**
- **Differential circuit has benefit of canceling noise and even-order nonlinear distortion**
- **Performance is limited by matching and functional asymmetry in the circuit,**
  - **bandgap, gm-C stages.**
- **Analog layout and routing should consider symmetry carefully.**

Signal-Path Devices

- **PMOS transistors have lower noise (whose mobility of holes is lower) comparing to NMOS**
  - **Avoid using NMOS transistors in the signal path**
- **Consider to use balanced/symmetric PMOS devices on the signal path.**
- **PMOS transistors should be referenced to clean analog supply voltage.**



- **NMOS transistors should be referenced to the substrate.**



A Sample Opamp for Simulation

CMOS Opamp with Sizing

A sample opamp

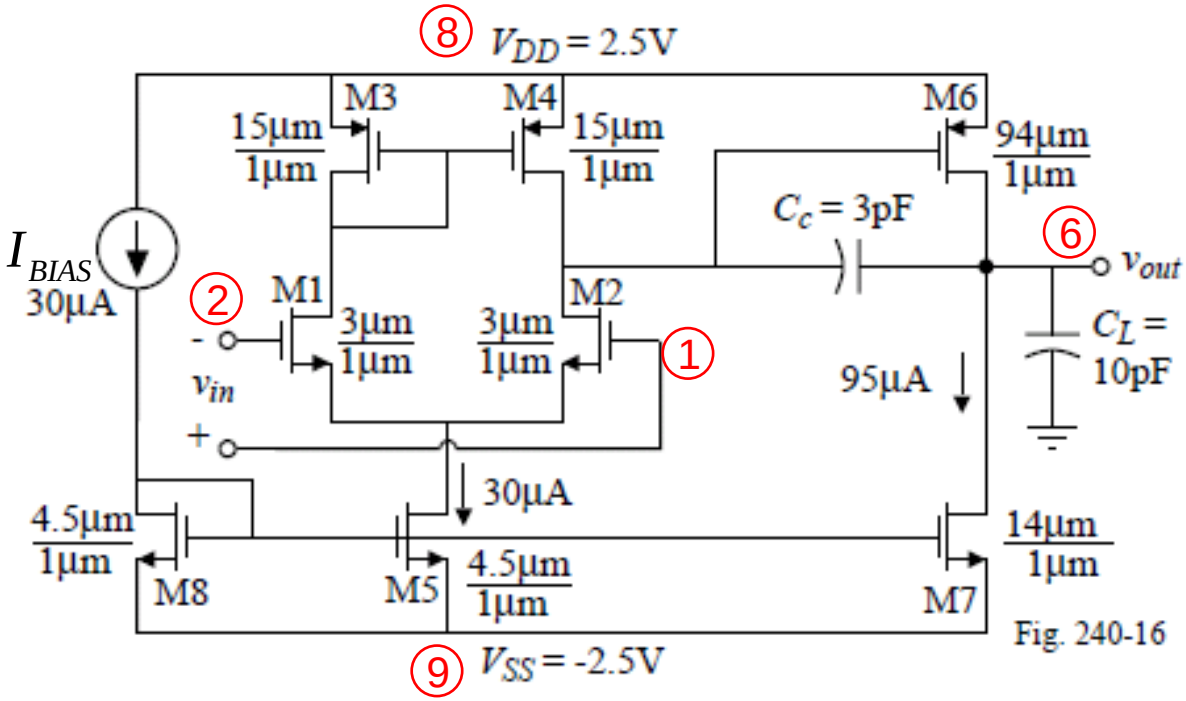
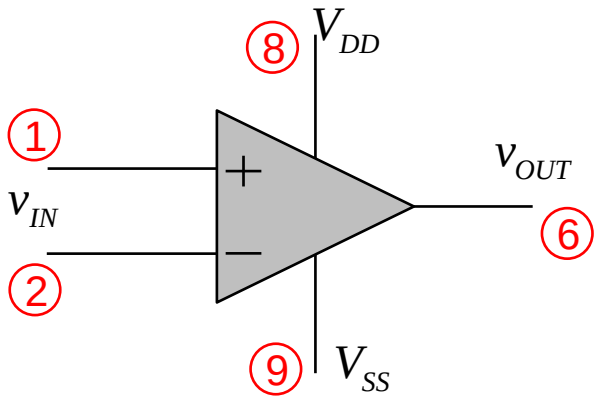


Fig. 240-16



Two-stage opamp with Miller compensation

Opamp Circuit

```
.SUBCKT OPAMP 1 2 6 8 9
M1 4 2 3 3 NMOS1 W=3U L=1U AD=18P AS=18P PD=18U PS=18U
M2 5 1 3 3 NMOS1 W=3U L=1U AD=18P AS=18P PD=18U PS=18U
M3 4 4 8 8 PMOS1 W=15U L=1U AD=90P AS=90P PD=42U PS=42U
M4 5 4 8 8 PMOS1 W=15U L=1U AD=90P AS=90P PD=42U PS=42U
M5 3 7 9 9 NMOS1 W=4.5U L=1U AD=27P AS=27P PD=21U PS=21U
M6 6 5 8 8 PMOS1 W=94U L=1U AD=564P AS=564P PD=200U PS=200U
M7 6 7 9 9 NMOS1 W=14U L=1U AD=84P AS=84P PD=40U PS=40U
M8 7 7 9 9 NMOS1 W=4.5U L=1U AD=27P AS=27P PD=21U PS=21U
CC 5 6 3.0P
.MODEL NMOS1 NMOS VTO=0.70 KP=110U GAMMA=0.4 LAMBDA=0.04 PHI=0.7
+MJ=0.5 MJSW=0.38 CGBO=700P CGSO=220P CGDO=220P CJ=770U CJSW=380P
+LD=0.016U TOX=14N
.MODEL PMOS1 PMOS VTO=-0.7 KP=50U GAMMA=0..57 LAMBDA=0.05 PHI=0.8
+MJ=0.5 MJSW=.35 CGBO=700P CGSO=220P CGDO=220P CJ=560U CJSW=350P
+LD=0.014U TOX=14N
IBIAS 8 7 30U
.ENDS
```

AD: Drain Area; PD: Drain Perimeter; (next page)

Assignment 1

- **Please simulate the sample opamp using your preferred simulator.**
- **Report the simulation results, including all modifications you made to the circuit.**
- **Also simulate the circuit in closed loop.**
- **Include both time-domain large-signal and frequency-domain small-signal simulation results.**
- **Due in one weak. Please prepare to present!**
- **Submit printed report for grading. Remember to put in your name and student ID#.**

References

1. **Prof. Yu, Sang Dae (劉尚大)'s Lecture, Kyungpook National University (韩国庆北大学), Integrated Systems Lab, School of Electronics Engineering, Taegu, Korea.**
2. **G. Palmisano, G. Palumbo, and S. Pennisi, "Design procedure for two-stage CMOS transconductance operational amplifiers: a tutorial," Analog Integrated Circuits and Signal Processing, vol. 27, pp. 179-189, 2001.**