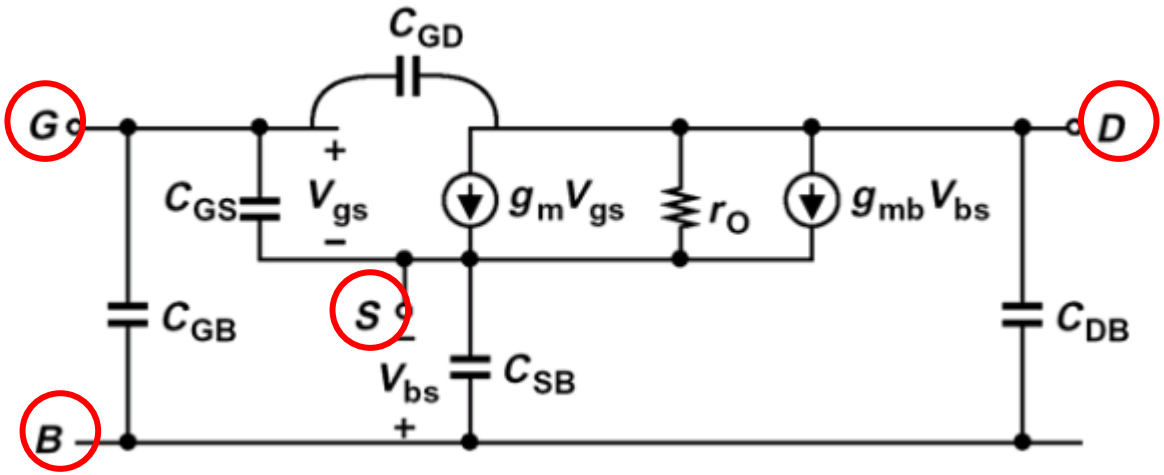
Lecture 5.
Pole/Zero Analysis of Two-Stage Amplifiers

Prof. Guoyong Shi
shiguoyong@sjtu.edu.cn
School of Micro/Nano-electronics
Shanghai Jiao Tong University
2015

Outline

- Small-signal MOS models
- Two-stage opamp small-signal model
- Two-pole analysis
- Deriving poles and zeros by DPI
- Frequency compensation
- Design for phase margin
- Pole/zero intuitions
- Design strategies for zero
  - Canceling the 2nd pole by zero
  - Adding gain to the compensation path

Small-signal MOS Model



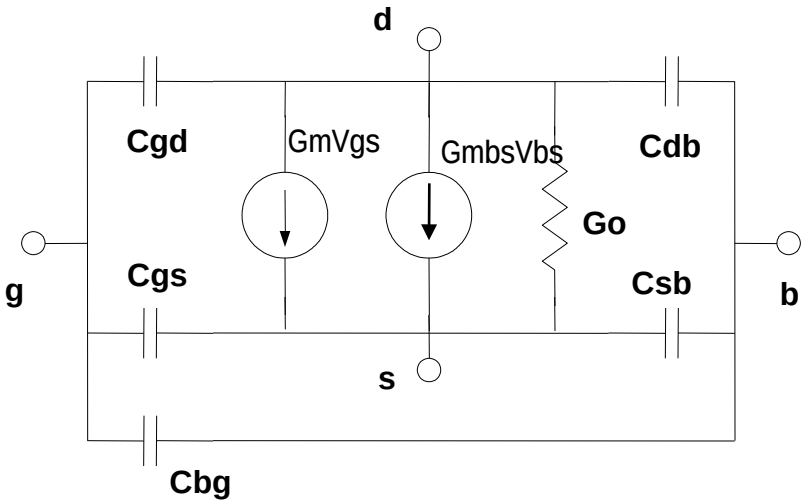
MOS Small-Signal Model

- G_m, G_{mb}, and G_o vary with the operation point.
- I_{ds} and V_{sb} are obtained by DC analysis.
- Other parameters are MOS device parameters.

$$g_o = \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{1}{\lambda I_{ds}}$$

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \sqrt{2kI_{ds}\frac{W}{L}}$$

$$g_{mb} = \frac{\partial I_{ds}}{\partial V_{bs}} = \frac{\gamma}{2\sqrt{2\phi_f + V_{sb}}} g_m$$



Level 2 MOS Small-Signal Model

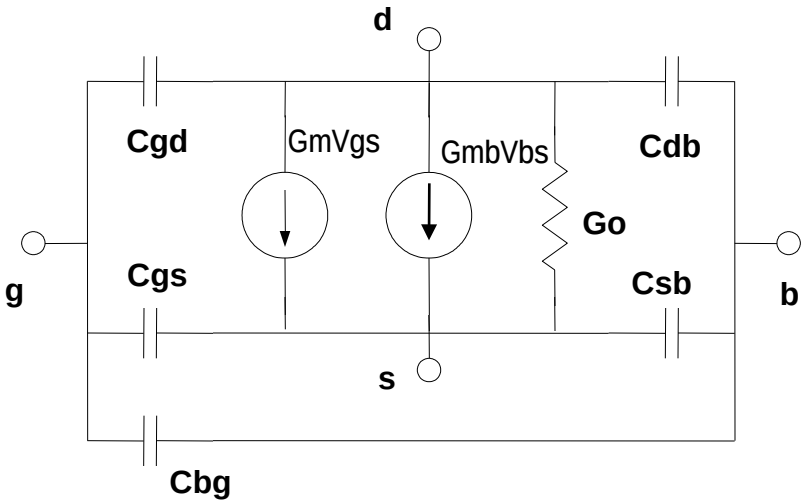
- **C_{GSO} and C_{ox} etc. are the MOS device parameter.**

$$C_{GS} = C_{GSo} + \frac{1}{2}C_{ox}$$

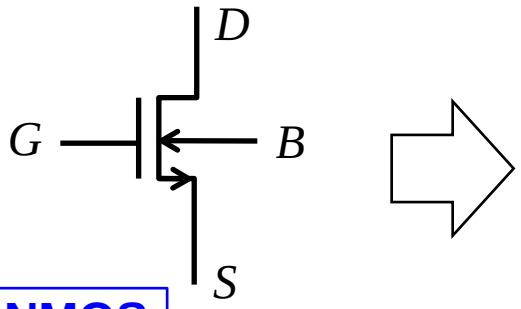
$$C_{GD} = C_{GDo} + \frac{1}{2}C_{ox}$$

$$C_{SB} = C_{JSB} + \frac{1}{2}C_{JBC}$$

$$C_{DB} = C_{JDB} + \frac{1}{2}C_{JBC}$$

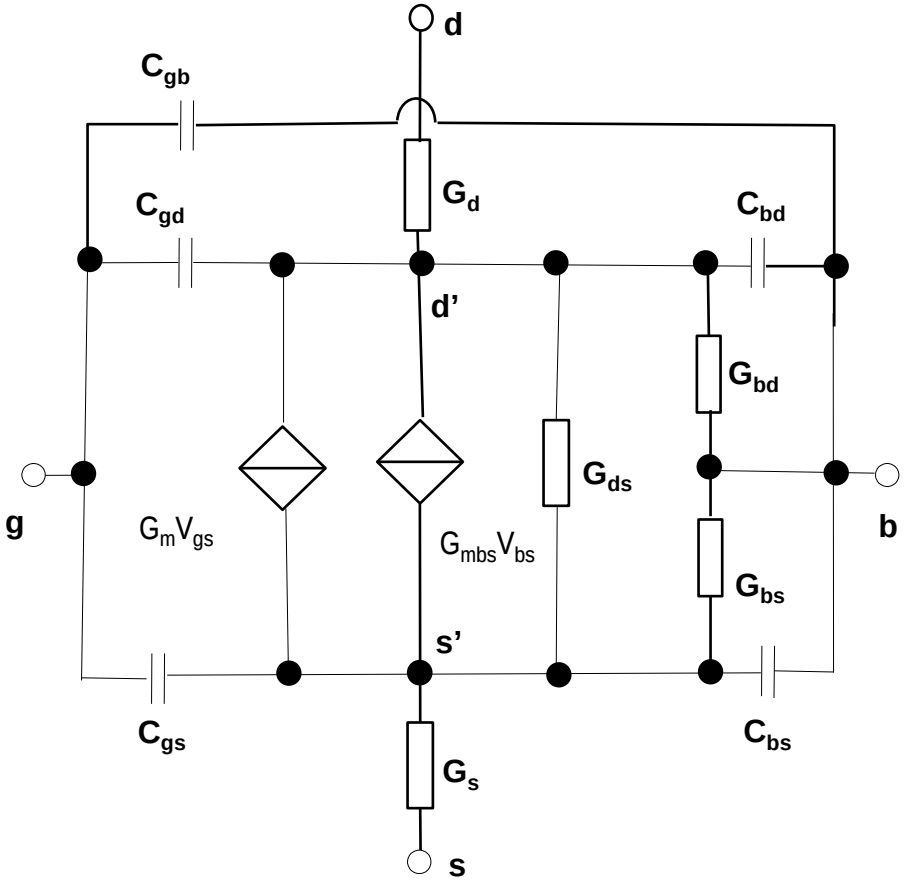


Level 3 MOS Small-Signal Model

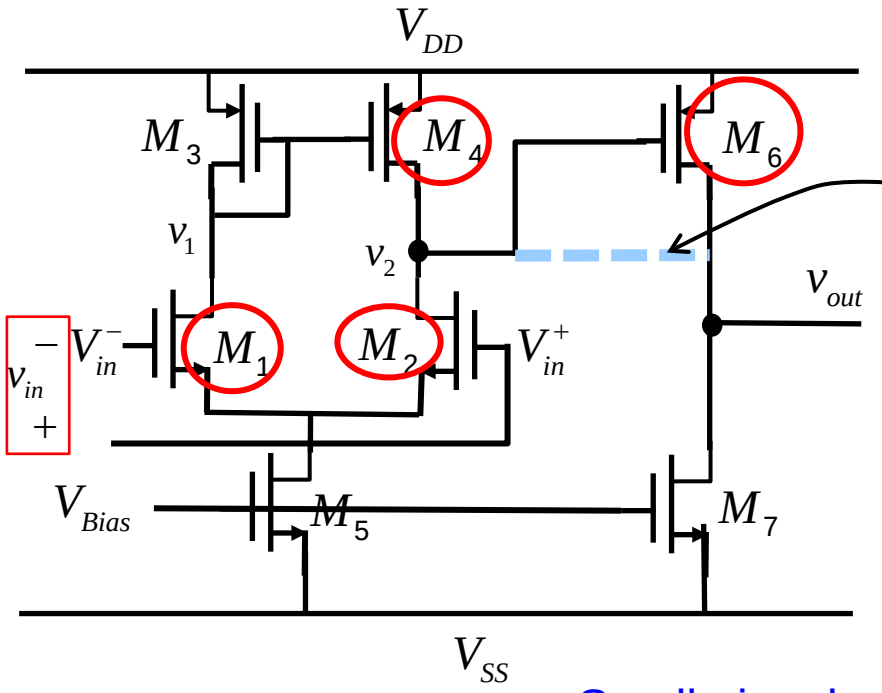


NMOS

#Cap = 5
#Res = 5
#VCCS = 2

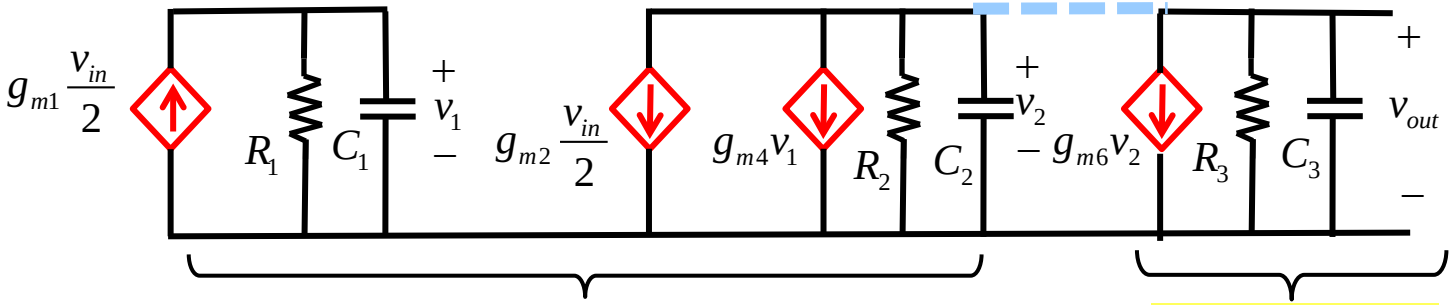


Two-Stage Opamp (uncompensated)

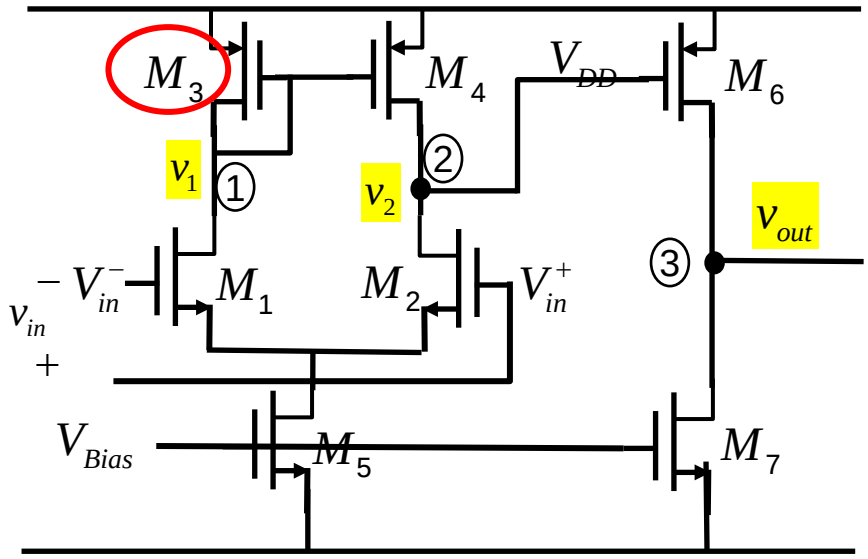


Compensation path

Small-signal model



Small-Signal Resistances



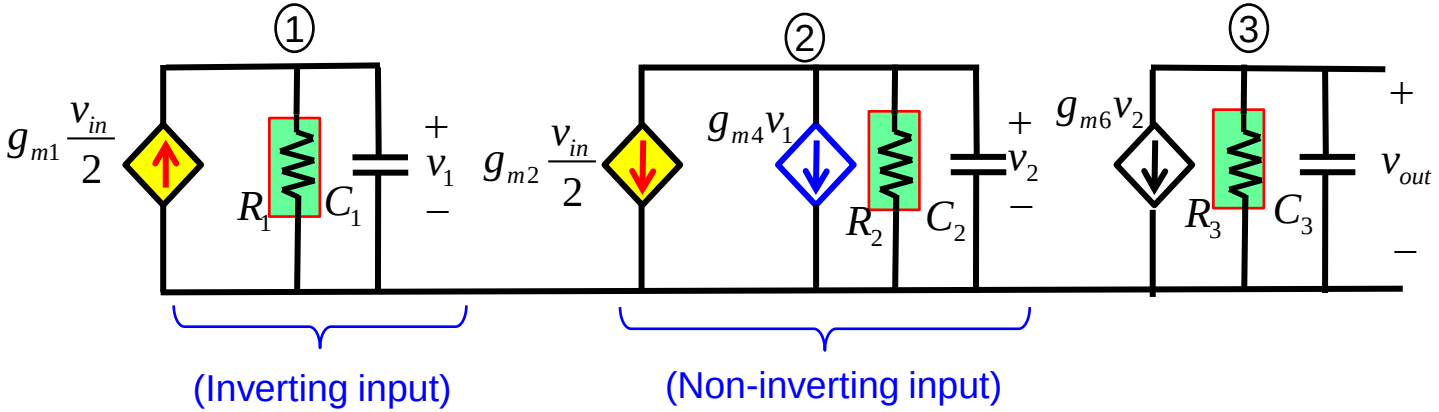
M3 diode connected

$$R_1 \approx r_{ds1} \parallel r_{ds3} \parallel \frac{1}{g_{m3}} \approx \frac{1}{g_{m3}}$$

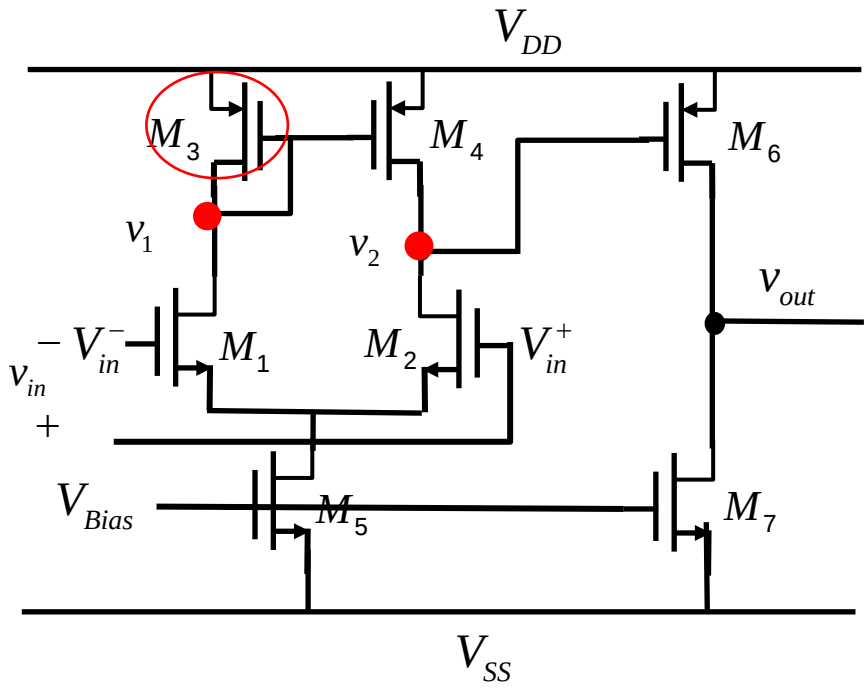
$$R_2 = r_{ds2} \parallel r_{ds4}$$

$$R_3 = r_{ds6} \parallel r_{ds7}$$

Small-signal model



Parasitic Capacitances



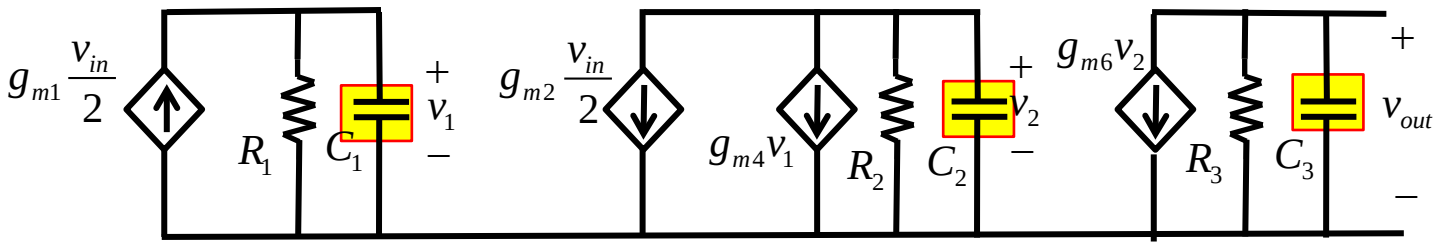
M3 diode connected

$$C_1 = C_{db1} + C_{gs3} + C_{db3} + C_{gs4}$$

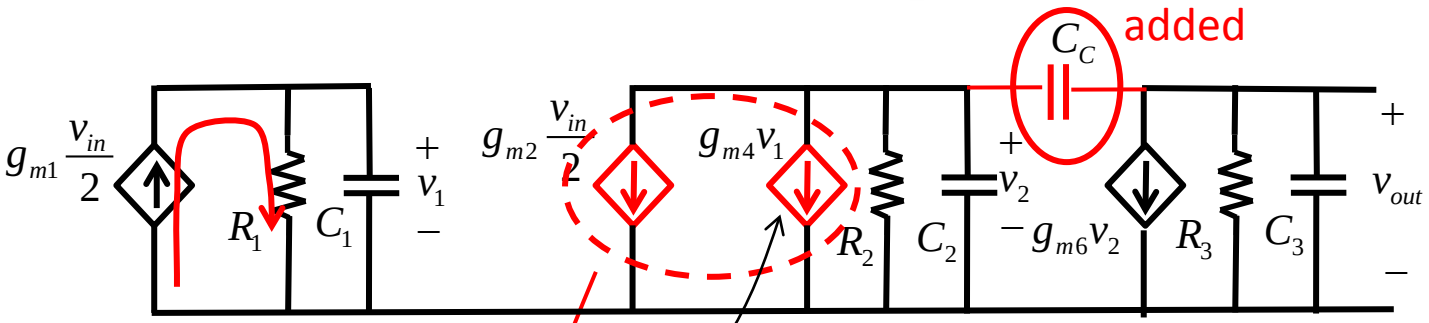
$$C_2 = C_{db2} + C_{db4} + C_{gs6}$$

$$C_3 = C_{bd6} + C_{bd7} + C_L$$

Small-signal model



Simplified small-signal model



$$R_2 = r_{ds2} \,||\, r_{ds4}$$

$$R_3 = r_{ds6} \,||\, r_{ds7}$$

Assume:

$$C_1 \approx 0;$$

$$v_1 = R_1 g_{m1} \frac{v_{in}}{2};$$

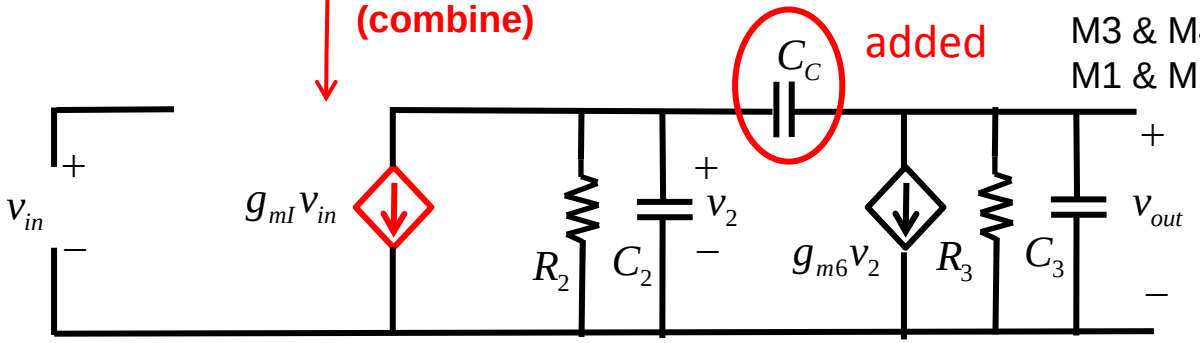
$$R_1 \approx \frac{1}{g_{m3}} \,||\, r_{ds1} \,||\, r_{ds3} \approx \frac{1}{g_{m3}}$$

(large)

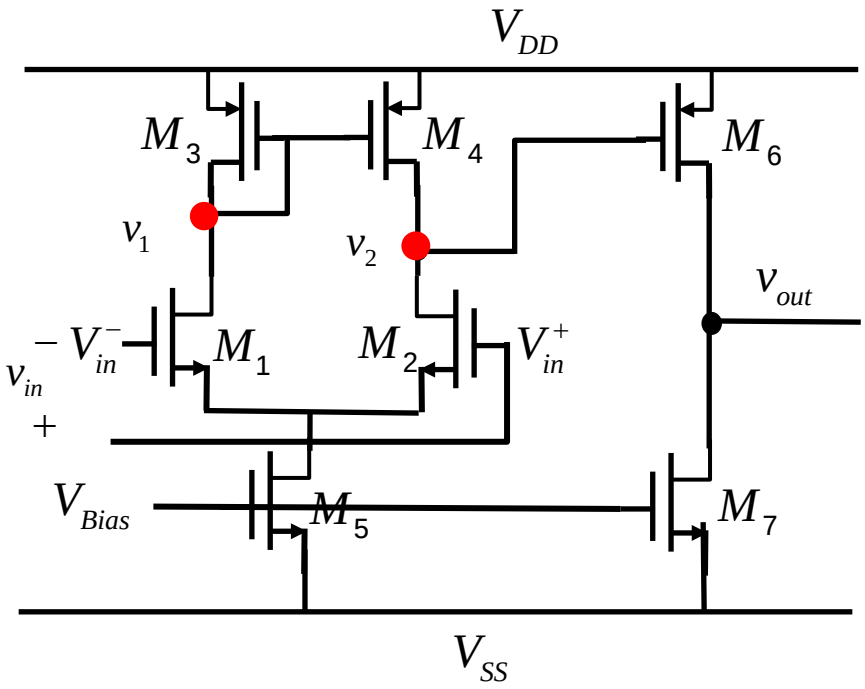
$$g_{m4}v_1 \approx g_{m4}\left(R_1 g_{m1}\frac{v_{in}}{2}\right) \approx g_{m4}\frac{1}{g_{m3}}g_{m1}\frac{v_{in}}{2} = g_{m1}\frac{v_{in}}{2}$$

(combine)

M3 & M4 are matched
M1 & M2 are matched



Simplified (Cont'd)



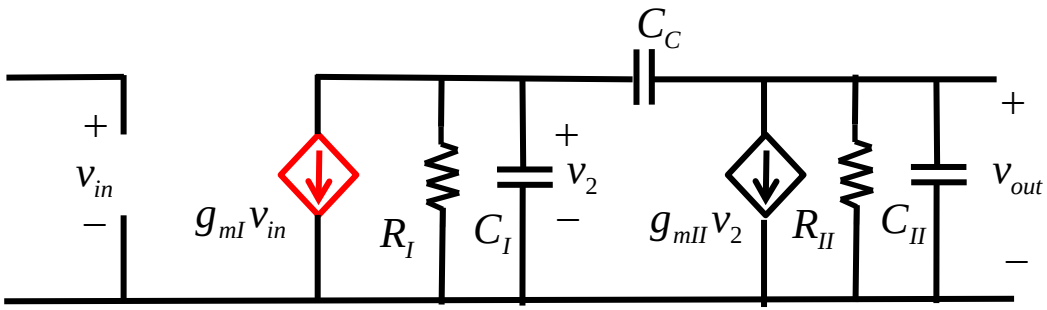
Subscripts I, II indicate the stages

$$g_{mI} = g_{m1} = g_{m2};$$

$$g_{mII} = g_{m6};$$

$$R_I = R_2 = r_{ds2} \parallel r_{ds4};$$

$$R_{II} = R_3 = r_{ds6} \parallel r_{ds7}$$



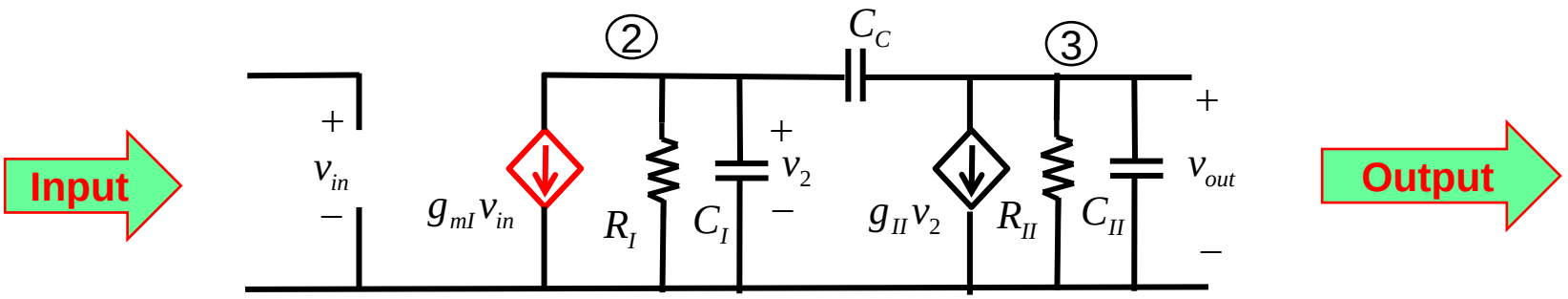
$$C_I = C_2 = C_{gs6} + C_{db2} + C_{db4}$$

$$C_{II} = C_3 = C_{db6} + C_{db7} + C_L \approx C_L$$

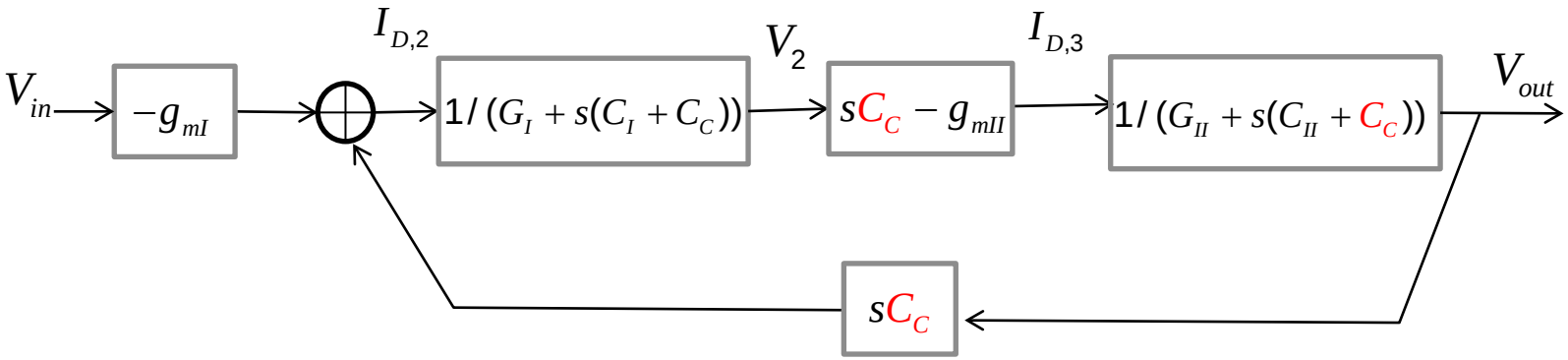
Assignment 2

- **Find the parasitic capacitances for the opamp circuit you used for SPICE simulation in the first assignment.**
- **Verify that the small-signal model has ac response close to the original circuit.**
- **Report any problems you have encountered.**

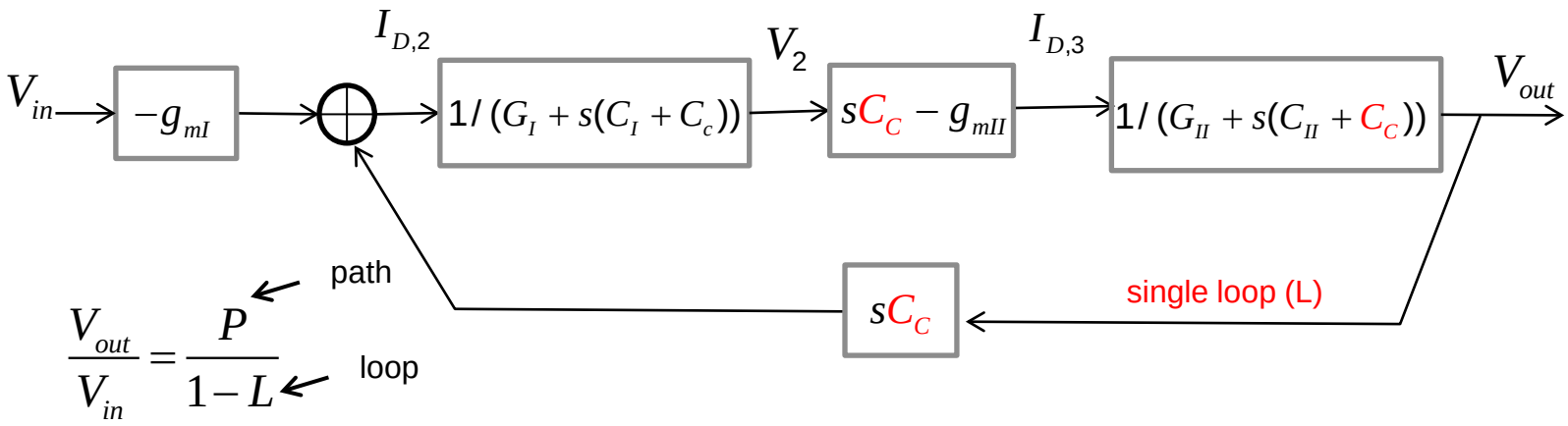
Driving Point Impedance (DPI)



To signal flow graph



DPI-SFG Analysis



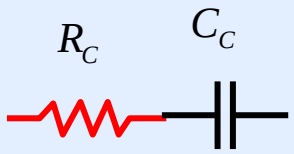
$$\frac{V_{out}}{V_{in}} = \frac{g_{mI}(g_{mII} - sC_C)}{[G_I + s(C_I + C_C)][G_{II} + s(C_{II} + C_C)] - sC_C(sC_C - g_{mII})}$$

$$= \frac{A_0[1 - s(C_C / g_{mII})]}{1 + s[R_{II}(C_{II} + C_C) + R_I(C_I + C_C) + R_I R_{II} g_{mII} C_C] + s^2 R_I R_{II}[C_I C_{II} + C_C(C_I + C_{II})]}$$

⇨ **dc gain** $A_0 = (R_I g_{mI})(R_{II} g_{mII})$ **one zero:** $z = \frac{g_{mII}}{C_C}$ rad/s

Exercise

Derive the expression for zero when a nulling resistor is added in the compensation path.



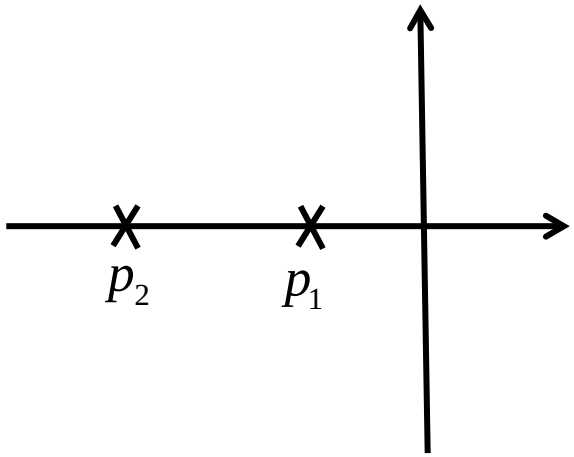
Poles

$$D(s)=\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)=1-s\left(\frac{1}{p_1}+\frac{1}{p_2}\right)+\frac{s^2}{p_1 p_2}$$

$$D(s)\approx 1-\frac{s}{p_1}+\frac{s^2}{p_1 p_2}$$

if $|p_2| >> |p_1|$

(widely separated)



Approximately determine p_1 and p_2 by comparing to the polynomial D(s):

$$D(s)=1+s\underbrace{[R_{II}(C_{II}+C_C)+R_I(C_I+C_C)+R_I R_{II} g_{mII} C_C]}_{-1/p_1}+s^2\underbrace{R_I R_{II}[C_I C_{II}+C_C(C_I+C_{II})]}_{1/p_1 p_2}$$

Finding the Poles

$$D(s) = 1 + s\underbrace{[R_{II}(C_{II}+C_C) + R_I(C_I+C_C) + R_I R_{II} g_{mII} C_C]}_{-1/p_1} + s^2 \underbrace{R_I R_{II}[C_I C_{II} + C_C(C_I + C_{II})]}_{1/p_1 p_2}$$

(Dominating term)

$$p_1 = -1/[R_{II}(C_{II}+C_C) + R_I(C_I+C_C) + R_I R_{II} g_{mII} C_C] \approx \frac{-1}{R_I R_{II} g_{mII} C_C}$$

(for g_{mII} large)

$$p_2 \approx \frac{-g_{mII} C_C}{C_I C_{II} + C_C(C_I + C_{II})} = \frac{-g_{mII} C_C}{(C_I + C_C)C_{II} + C_C C_I} \approx \frac{-g_{mII}}{C_{II}}$$

$C_{II} >> C_I$

Note that the units of p1, p2 are rad/s

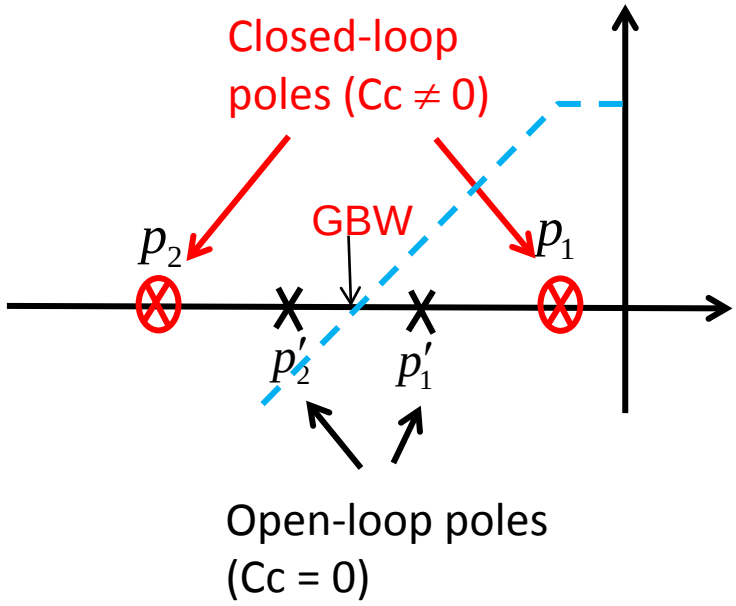
Please take a look what transistors are related to these two poles?

The 2nd Pole

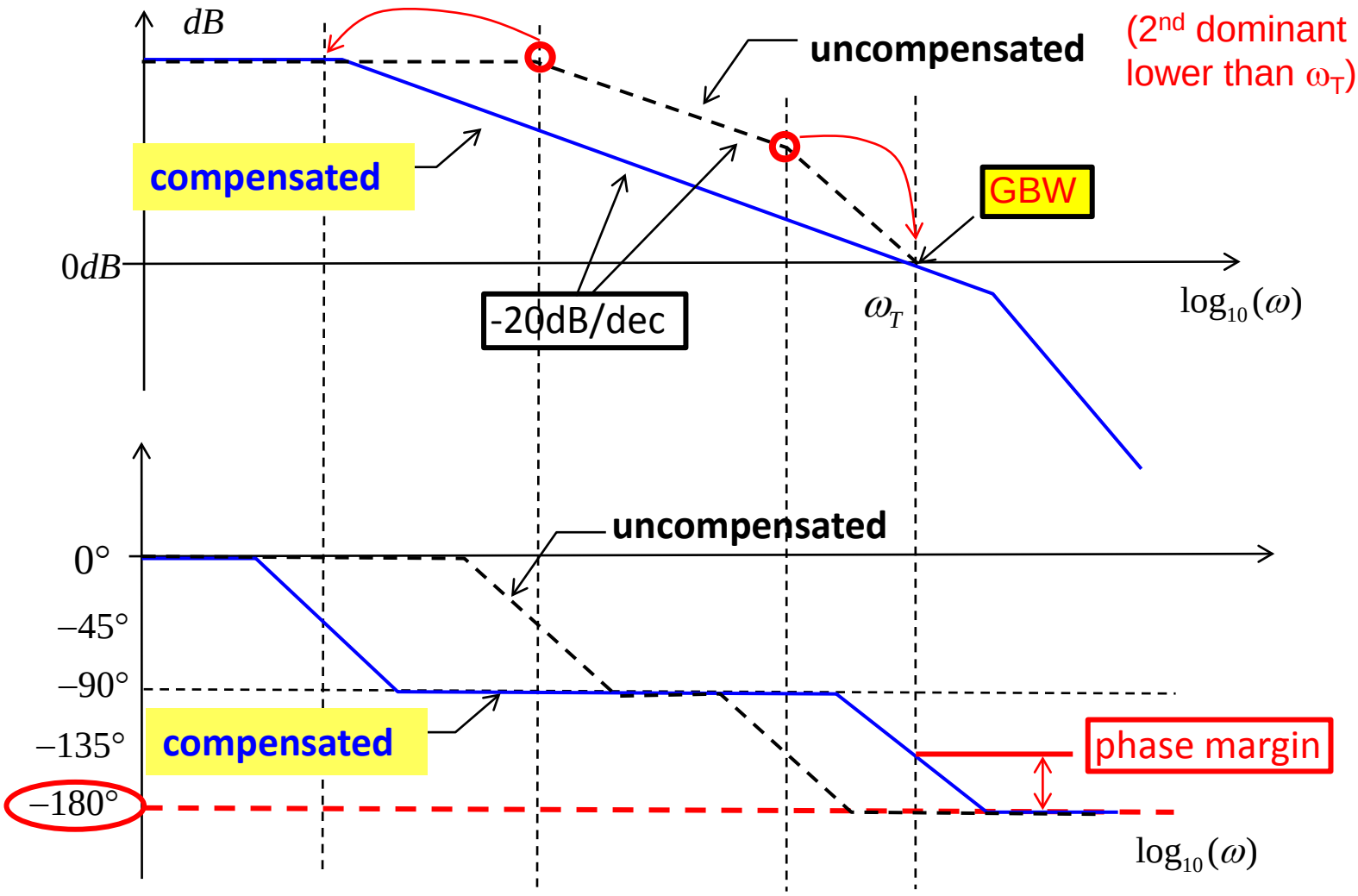
$$p_2 \approx \frac{-g_{mII}C_C}{C_I C_{II} + C_C(C_I + C_{II})} \approx -\frac{g_{mII}}{C_{II}}$$

$C_{II} >> C_C > C_I$

The **2nd pole** must be greater than GBW. Otherwise the phase margin might not be satisfied.



Frequency Compensation



Gain-Bandwidth Product (GBW)

(dominant)

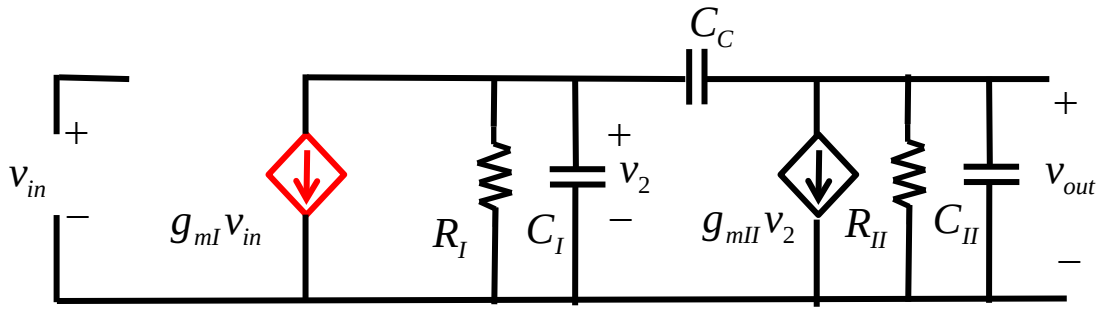
$$p_1 = -1/[R_{II}(C_{II}+C_C)+R_I(C_I+C_C)+R_I R_{II} g_{mII} C_C] \approx \frac{-1}{R_I R_{II} g_{mII} C_C}$$

$$A_0 = (R_I g_{mI})(R_{II} g_{mII}) \qquad \textbf{(dc gain)}$$

$$\Rightarrow \quad GBW = A_0 |p_1| = \frac{(R_I g_{mI})(R_{II} g_{mII})}{R_I R_{II} g_{mII} C_C} = \frac{g_{mI}}{C_C} = \frac{g_{m1}}{C_C}$$

$$GBW = \frac{g_{m1}}{C_C}$$

Zero & Poles



$$R_I = R_2 = r_{ds2} \parallel r_{ds4}; \qquad R_{II} = R_3 = r_{ds6} \parallel r_{ds7} \qquad g_{mII} = g_{m6};$$

Zero:

$$z = \frac{g_{mII}}{C_C} = \frac{g_{m6}}{C_C}$$

Poles:

$$p_1 \approx \frac{-1}{R_I R_{II} g_{mII} C_C} = \frac{-(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}{g_{m6} C_C}$$

g_{mII} large

$$p_2 \approx \frac{-g_{mII} C_C}{C_I C_{II} + C_C (C_I + C_{II})} \approx \frac{-g_{mII}}{C_{II}} \approx \frac{-g_{mII}}{C_L}$$

$C_{II} > C_C > C_I$

The output load C_L affects the 2nd pole.

Phase Margin

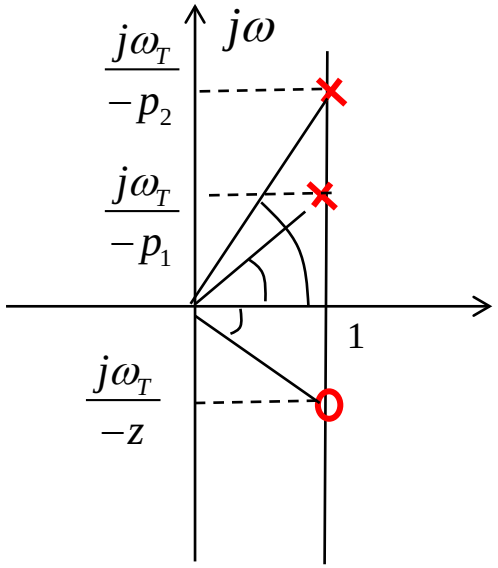
Open-loop transfer function H(s):

$$H(s)=\frac{A_0(1-s/z)}{(1-s/p_1)(1-s/p_2)} \qquad z>0; \qquad p_{1,2}<0$$

Phase:

$$\angle H(s)=\angle(1-s/z)-\angle(1-s/p_1)-\angle(1-s/p_2)$$
$$=\varphi_z-\varphi_{p1}-\varphi_{p2}\in(0°,-180°)$$

$$s=j\omega_T=jGBW$$



Suppose you want at least 45° phase margin:

$$\varphi_z-\varphi_{p1}-\varphi_{p2}>-180°+45°=-135°$$

$$\Rightarrow \quad -\varphi_z+\varphi_{p1}+\varphi_{p2}<135°$$

$$\Rightarrow \quad \tan^{-1}\frac{\omega_T}{z}+\tan^{-1}\frac{\omega_T}{|p_1|}+\tan^{-1}\frac{\omega_T}{|p_2|}<135°$$

(The zero could be + or –.
A + zero worsens PM. Hence, called "non-minimum phase zero".)

Design for Phase Margin

Placement of zero

$$z > 10 \cdot GBW \Leftrightarrow \frac{g_{m6}}{C_C} > \frac{10 g_{m1}}{C_C} \Leftrightarrow g_{m6} > 10 g_{m1}$$

Reference for sizing!

$$\arctan\frac{GBW}{|z|} + \arctan\frac{GBW}{|p_1|} + \arctan\frac{GBW}{|p_2|} < 135°$$

large

$$GBW = A_0 \cdot |p_1|$$

$$\Rightarrow \quad \operatorname{atan}(0.1) + 90° + \operatorname{atan}\left(\frac{GBW}{|p_2|}\right) < 135°$$

$$\Rightarrow \quad \operatorname{atan}\left(\frac{GBW}{|p_2|}\right) < 45° - 5.7° = 39.3° \quad \Rightarrow \quad |p_2| \geq 1.22 GBW$$

Phase Marge (Alternative)

Alternatively, you may use other estimates to place the 2nd pole.

For example, the CL also affects p2, hence the phase margins.

$$C_C > 0.22C_{II} \Rightarrow |p_2| = \frac{g_{m6}}{C_{II}} > \frac{10g_{m1}}{C_{II}} > \frac{2.2g_{m1}}{C_C} = 2.2GBW$$

$$\Rightarrow |p_2| \geq 2.2GBW$$

Pole/Zero Intuitions

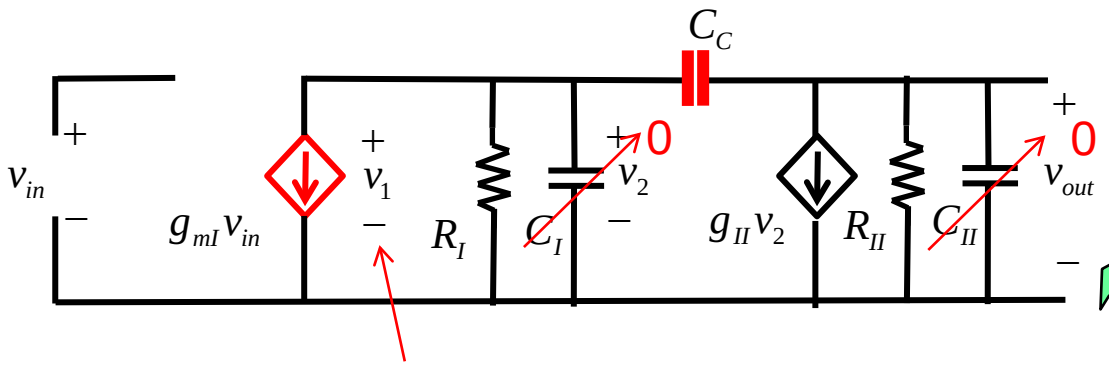
- **Dominant pole**
- **Miller theorem**

The Dominant Pole

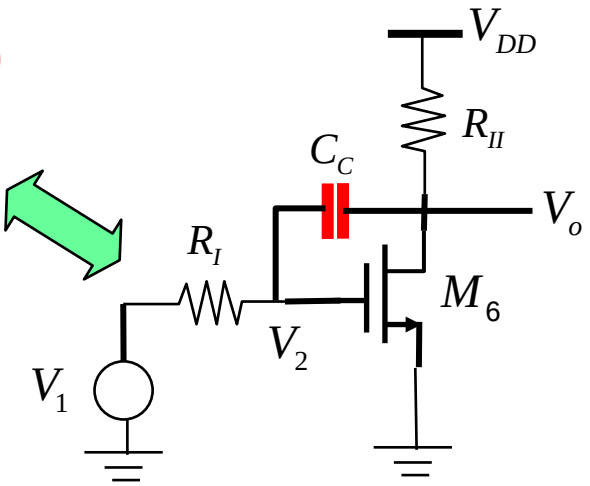
$$p_1 \approx \frac{-1}{R_I R_{II} g_{mII} C_C} = \frac{-1}{R_I \underbrace{[g_{mII} R_{II} C_C]}_{\text{Miller cap}}}$$

g_{mII} large

The dominant pole (p1) only depends on R_I, R_{II}, g_{mII}, and C_C, which is the pole of the following small-signal circuit:

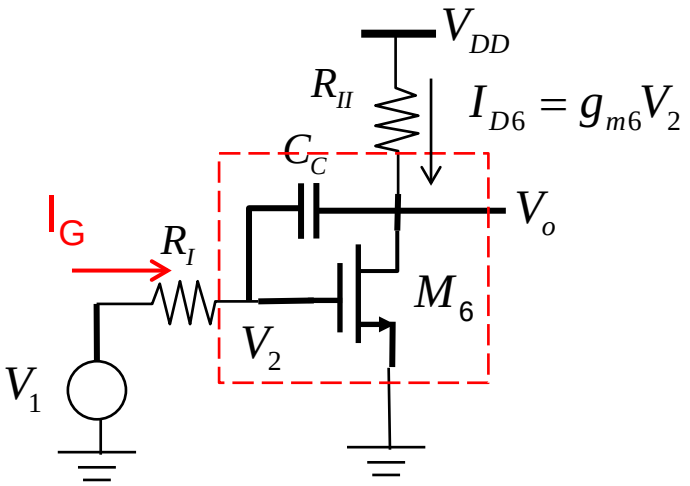


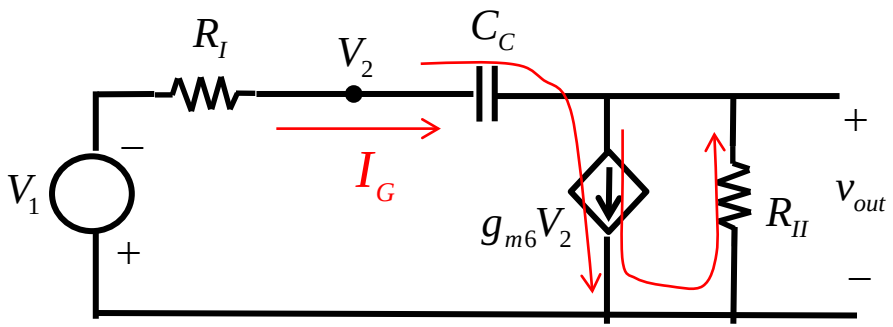
Consider v1 as input



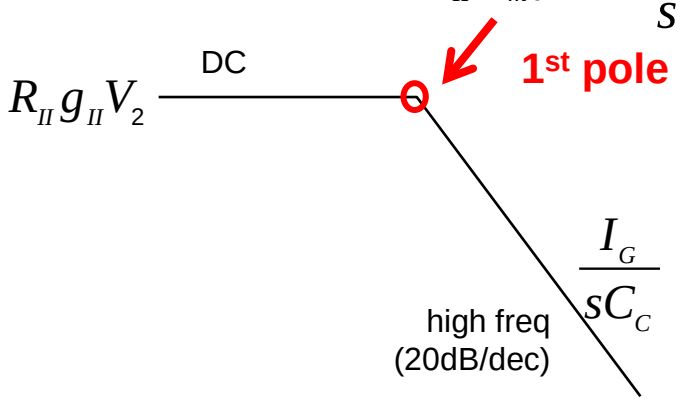
Equiv. circuit

Approximate Treatment





$$R_{II} g_{m6} V_2 = \frac{I_G}{sCc}$$



- **At DC:**

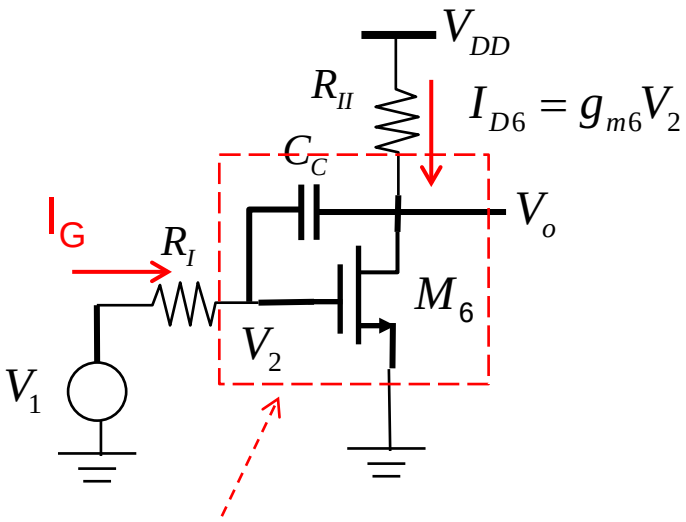
$$V_{out} = R_{II} g_{II} V_2$$

- **This circuit has a zero. Before reaching zero (ωCc < gm6), the voltage drop at Cc dominates the output.**

$$V_{out} = V_2 + \frac{I_G}{sC_C} \approx \frac{I_G}{sC_C}$$

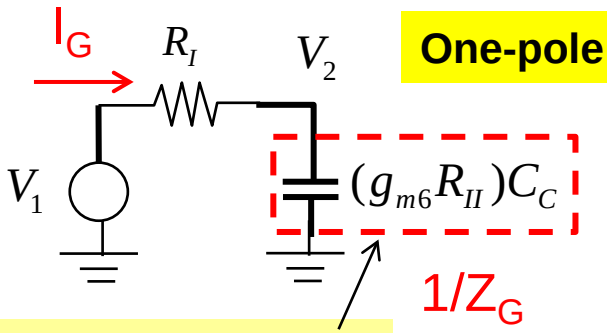
One-pole Model

$$R_{II} g_{m6} V_2 = \frac{I_G}{sC_C}$$



Z_G: impedance seen by I_G

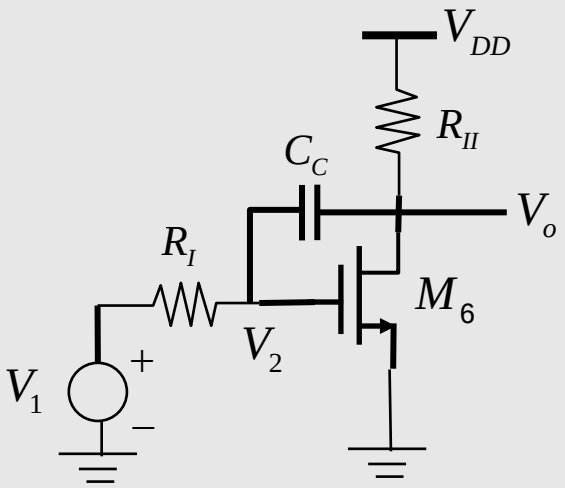
$$Z_G \equiv \frac{V_2}{I_G} = \frac{1}{sC_C g_{m6} R_{II}}$$



One-pole model

Cap amplified by ($g_{m6}R_{II}$)

Exercise



Derive the exact voltage transfer function by the DPI method.

$$\frac{V_o}{V_1} = \frac{(R_{II} g_{m6})[1 - s(C_C / g_{m6})]}{1 + sC_C \left(R_I + R_{II} + R_I R_{II} g_{m6} \right)}$$

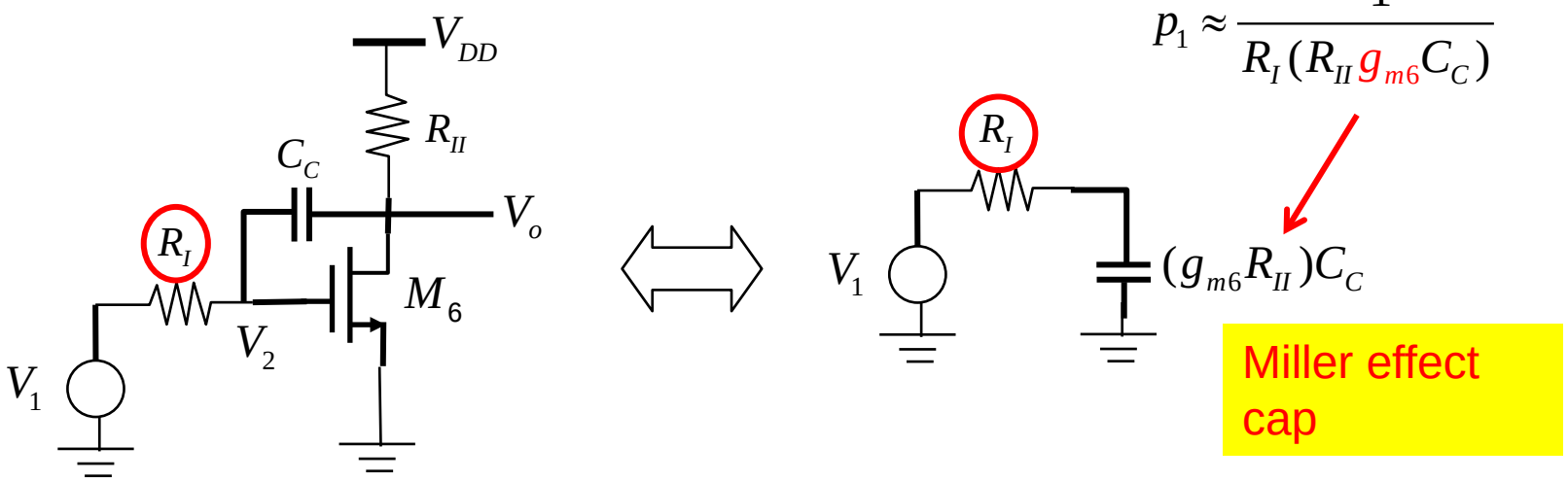
Has a zero z and a pole p, |z| > |p|.

Dominant Pole

$$\frac{V_o}{V_1} = \frac{(R_{II} g_{mII})[1 - s(C_C / g_{mII})]}{1 + sC_C\left(R_I + R_{II} + R_I R_{II} g_{mII}\right)}$$

Dominant pole

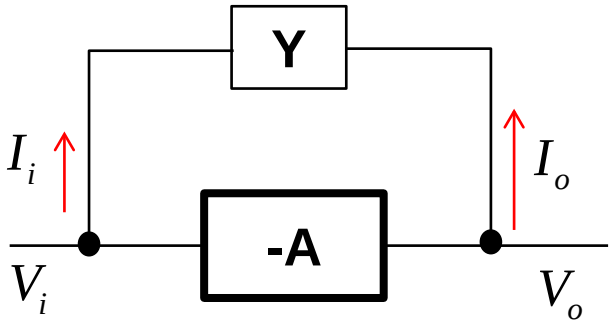
$$p_1 \approx \frac{-1}{R_I (R_{II} g_{m6} C_C)}$$



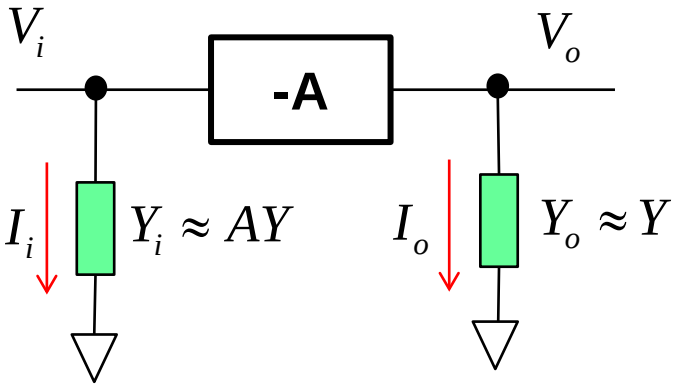
Miller effect cap

Miller Theorem

Redistributing the feedback admittance to the two terminals ...



Equiv



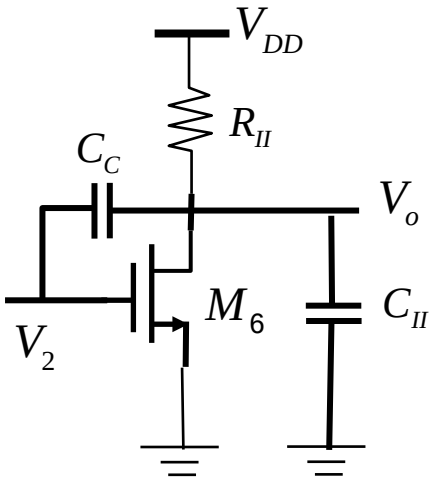
Proof

$$V_o = -AV_i; \qquad A \gg 1$$

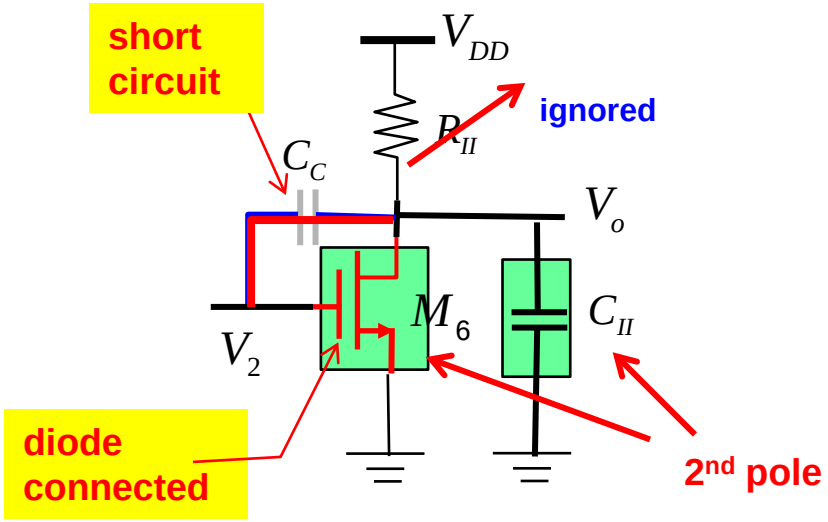
$$\begin{cases} I_i = Y(V_i - V_o) = Y(1+A)V_i \approx YAV_i; \quad I_i = Y_i V_i \\ I_o = Y(V_o - V_i) = Y(1+\frac{1}{A})V_o \approx YV_o; \quad I_o = Y_o V_o \end{cases} \Rightarrow \begin{cases} Y_i \approx AY \\ Y_o \approx Y \end{cases}$$

Intuition of the 2nd Pole

At high freq, Cc is roughly short circuited, M6 is almost *diode connected*.



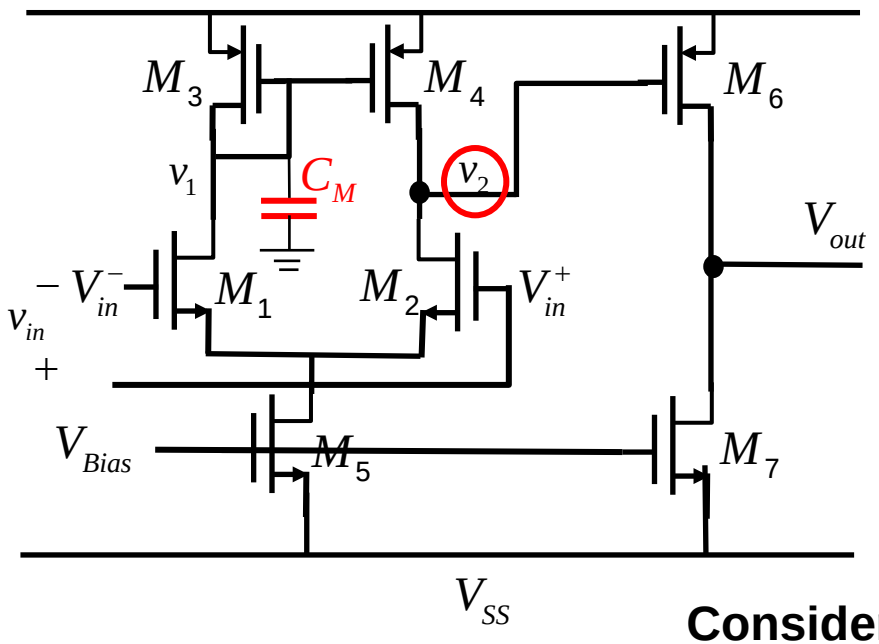
$C_{II} > C_C > C_I$



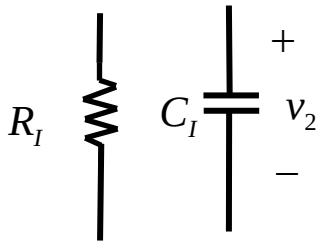
$$p_2 \approx \frac{-g_{mII}}{C_{II}}$$

(indep of Cc & R_{II})

The Mirror Pole



C_M is the parasitic cap of the 1st stage mirror (it contributes to the **mirror pole**).

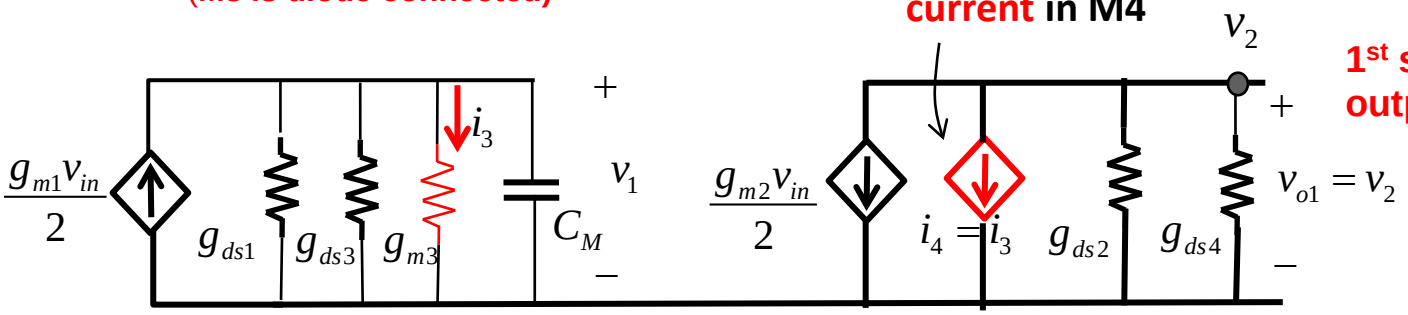


Consider transfer from v_{in} to v_2.

(M3 is diode connected)

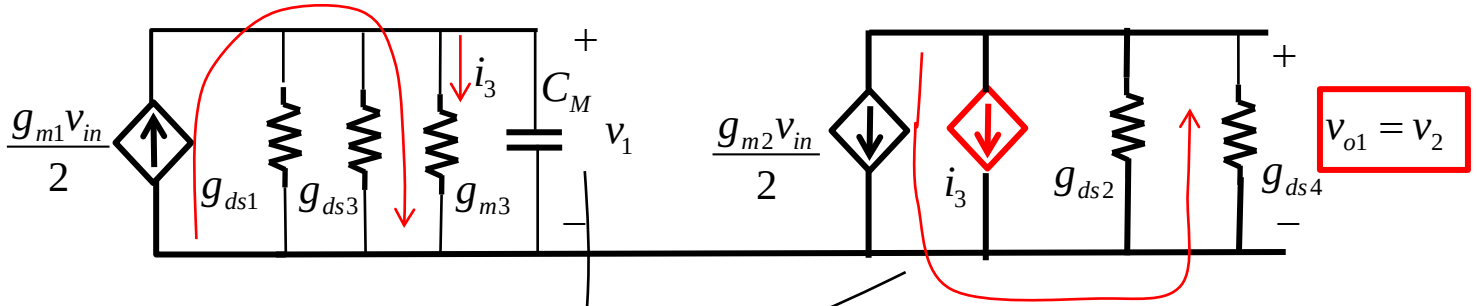
mirrored current in M4

1st stage output



Mirror Pole (cont'd)

Consider transfer from v_{in} to v_2.



$$v_2 = -\left[i_3 + \frac{g_{m2}v_{in}}{2} \right] \frac{1}{g_{ds2} + g_{ds4}}$$

$$= -\left[g_{m3}v_1 + \frac{g_{m2}v_{in}}{2} \right] \frac{1}{g_{ds2} + g_{ds4}}$$

$$= -\left[g_{m3} \frac{g_{m1}v_{in}}{2(g_{ds1} + g_{ds3} + g_{m3} + sC_M)} + \frac{g_{m2}v_{in}}{2} \right] \frac{1}{g_{ds2} + g_{ds4}} \qquad (g_{m1} = g_{m2})$$

$$= -\frac{g_{m1}}{2(g_{ds2} + g_{ds4})} \left[\frac{g_{m3}}{g_{ds1} + g_{ds3} + g_{m3} + sC_M} + 1 \right] v_{in}$$

small

$$\approx -\frac{g_{m1}}{2(g_{ds2} + g_{ds4})} \left(\frac{2g_{m3} + sC_M}{g_{m3} + sC_M} \right) v_{in}$$

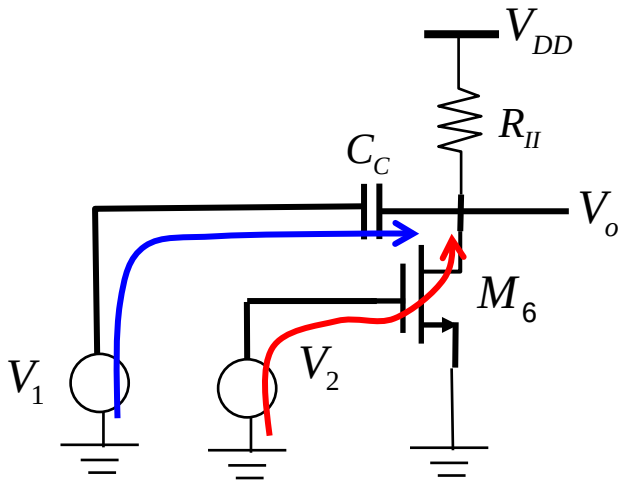
These two roots are much larger (>> GBW) ➔ their influence can be ignored.

Mirror zero: $z_M = -\frac{2g_{m3}}{C_M}$

Mirror pole: $p_M = -\frac{g_{m3}}{C_M}$

Zero Intuition

Zero always arises from superposition of **multiple paths** from the input to output.



$$V_{o,1} = \frac{R_{II}}{(R_{II} + 1/sC_C)} V_1$$

R_{II} and Cc in series when driven by V_1

$$V_{o,2} = \frac{R_{II} / sC_C}{(R_{II} + 1/sC_C)} (-g_{m6}) V_2$$

R_{II} and Cc in parallel when driven by V_2

$$V_o = V_{o,1} + V_{o,2} = \frac{R_{II}}{(R_{II} + 1/sC_C)} V_1 + \frac{R_{II} / sC_C}{(R_{II} + 1/sC_C)} (-g_{m6}) V_2$$

Assuming $V_1 = V_2$

$$= \frac{R_{II}(1 - g_{m6}/sC_C)}{(R_{II} + 1/sC_C)} V_1$$

zero

$$z = \frac{g_{m6}}{C_C}$$

The Issue of Zero

A positive zero **boosts the magnitude** but **lags the phase,**
– i.e., adding negative phase to reduce the phase margin

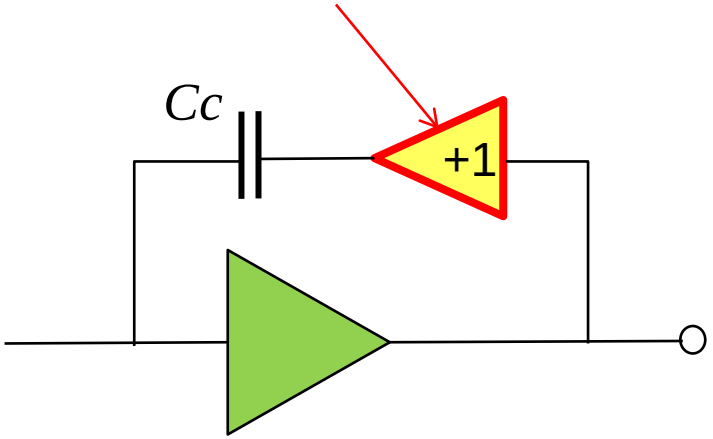
Design Guide:
If the **zero is caused by two paths**, try to eliminate one path.

Design Strategies for Zero

- **Adding buffer to compensation path**
- **Adding output resistance of buffer**
- **Adding nulling zero**

Strategy 1

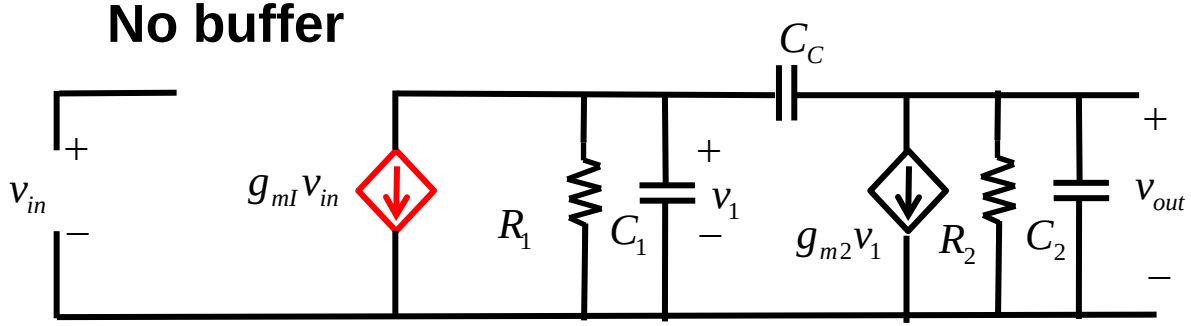
Adding buffer to break the compensation path



The **poles** are approximately **unchanged** (as if no buffer has been inserted).

Pole Analysis

No buffer

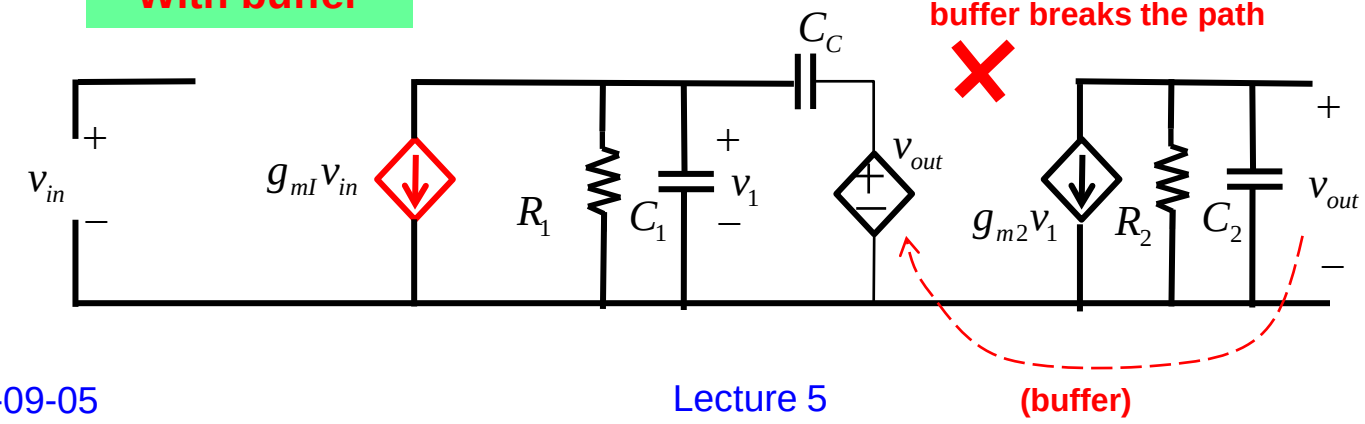


The two poles are unchanged

$$p_1 \approx \frac{-1}{g_{m2}R_1R_2Cc} \qquad p_2 \approx \frac{-g_{m2}Cc}{C_2(C_1+Cc)}$$

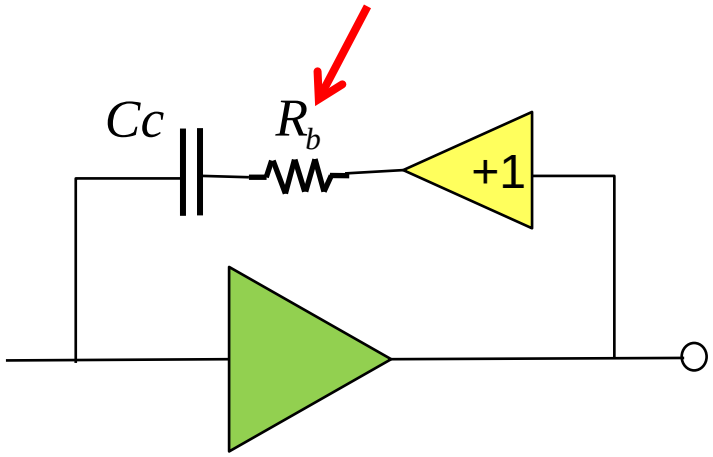
With buffer

buffer breaks the path



Strategy 2

Adding output resistance to buffer (R_b)



A new pole appears at

$$p_4 \approx \frac{-1}{R_b C_1 C_2 / (C_1 + Cc)}$$

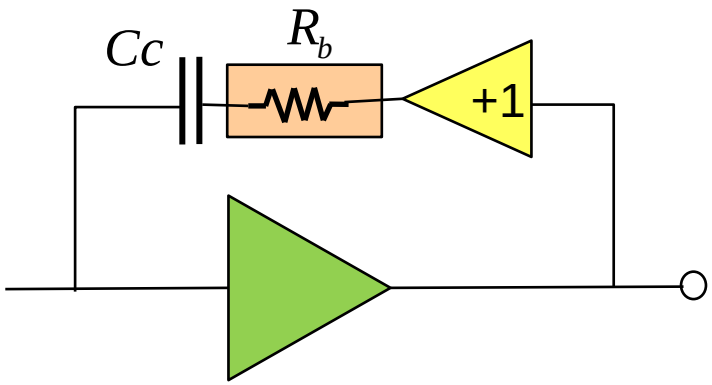
and additional LHP zero at

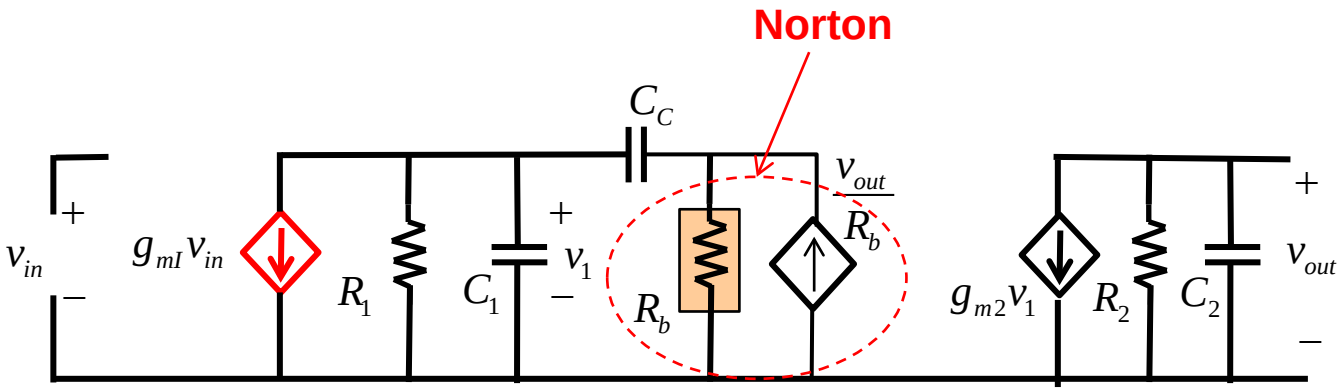
$$z_2 = \frac{-1}{R_b Cc}$$

The **nulling resistor** placed in series with Cc can eliminate the RHP zero or move it to the LHP.

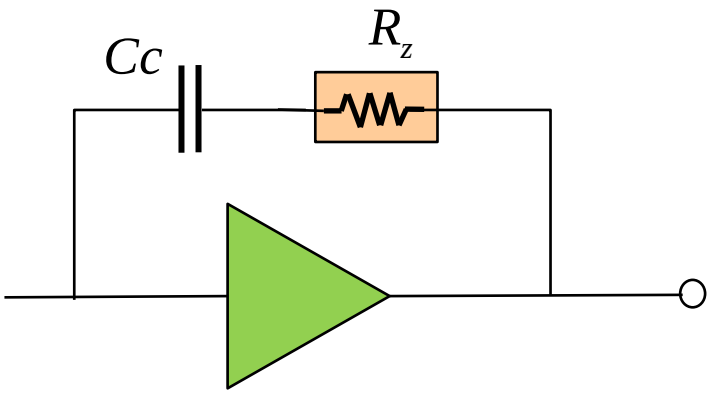
Exercise

Exercise: Derive poles-zeros for this circuit.

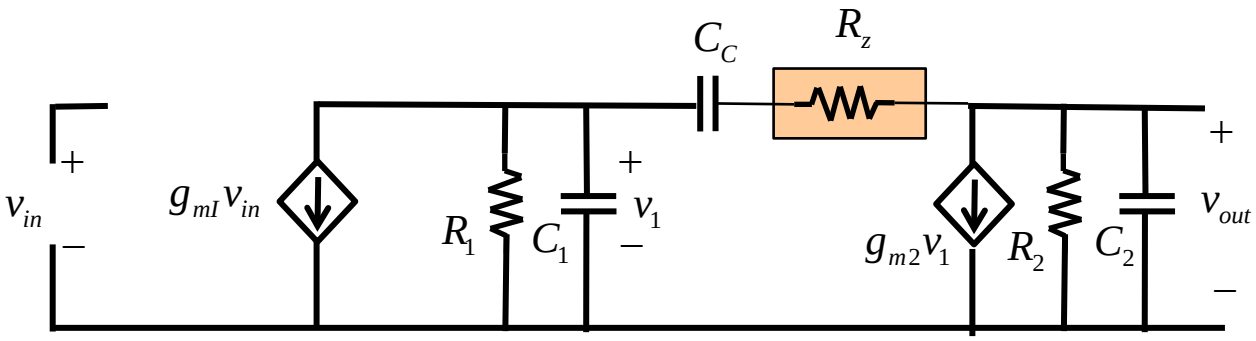




Strategy 3: Nulling Resistor



$$\frac{V_{out}}{V_{in}} = \frac{a\left\{1 - sCc\left[1/g_{m2} - R_z\right]\right\}}{1 + bs + cs^2 + ds^3}$$



Exercise

Exercise: Derive the poles/zeros by DPI analysis.

$$\frac{V_{out}}{V_{in}} = \frac{a\left\{1 - sCc\left[1/g_{m2} - R_z\right]\right\}}{1 + bs + cs^2 + ds^3}$$

It becomes a 3rd order system

where the coefficients are:

$$a = g_{mI} g_{mII} R_I R_{II}$$

denominator

$$b = (C_{II} + C_C)R_{II} + (C_I + C_C)R_I + g_{mII} R_I R_{II} C_C + R_z C_C$$

$$c = R_I R_{II}(C_I C_{II} + C_C C_I + C_C C_{II}) + R_z C_C (R_I C_I + R_{II} C_{II})$$

$$d = R_I R_{II} R_z C_I C_{II} C_C \quad \leftarrow \text{(3rd order coeff)}$$

Note: subscripts I, II indicate stages 1 and 2.

Poles and Zero with nulling Rz

Assume **Rz is less than R_I or R_{II}** and the **poles are widely spaced**, then the roots are

$$p_1 = \frac{-1}{(1+g_{mII}R_{II})R_I C_C} \approx \frac{-1}{R_I C_C (g_{mII}R_{II})}$$

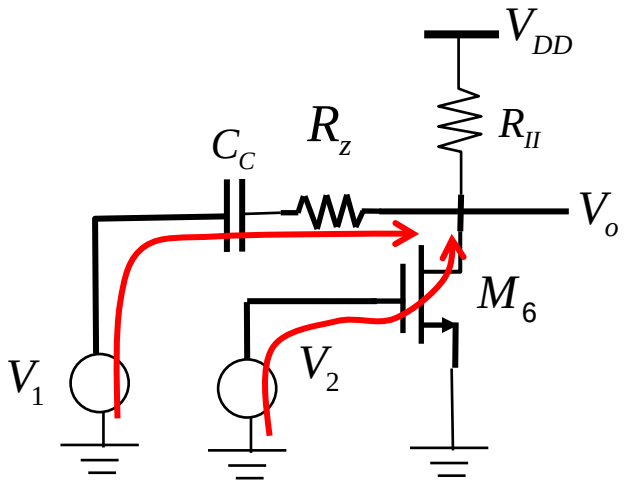
Exercise: Derive the poles and zero.

$$p_2 = \frac{-g_{mII}C_C}{C_I C_{II} + C_I C_C + C_{II} C_C} \approx \frac{-g_{mII}}{C_{II}}$$

$$p_3 = \text{mirror pole}$$

$$p_4 = \frac{-1}{R_z C_I} \qquad z_1 = \frac{1}{C_C\left(\frac{1}{g_{mII}} - R_z\right)} \approx \frac{1}{-C_C R_z} \qquad \left(\text{if } g_{mII}R_z \gg 1\right)$$

Conceptual Illustration



$$V_{out} = \frac{R_{II}}{(R_{II} + R_z + 1/sC_C)} V_1 + \frac{(-g_{m6})R_{II}(R_z + 1/sC_C)}{(R_{II} + R_z + 1/sC_C)} V_2$$

$$= \frac{R_{II}(1 - g_{m6}R_z - g_{m6}/sC_C)}{(R_{II} + R_z + 1/sC_C)} V_1$$

Assuming V1 = V2

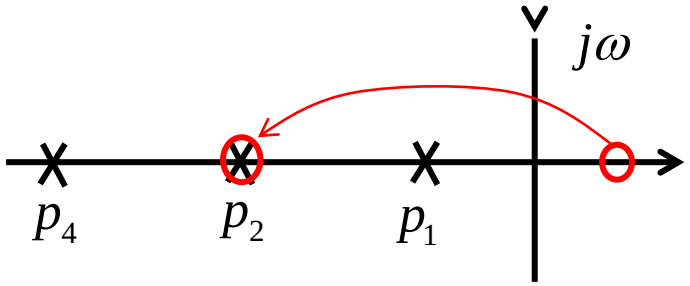
Assuming $g_{m6} = g_{mII}$, we get the zero as

$$z_1 = \frac{1}{C_C(1/g_{mII} - R_z)}$$

Zero Cancellation

If we place **z1 = p2**, i.e., let **the zero cancel the 2nd pole**.

$$\frac{1}{C_C(1/g_{mII} - R_z)} = \frac{-g_{mII}}{C_{II}}$$



$$\Rightarrow \quad R_z = \frac{(C_C + C_{II})}{g_{mII} C_C}$$

With **p2 canceled**, the remaining roots **are p1 and p4 (p4 due to Rz)**. For unity-gain stability, it is required that

$$|p_4| > GBW = A_0 |p_1| = \frac{A_0}{g_{mII} R_I R_{II} C_C} = \frac{g_{mI}}{C_C} \quad \Rightarrow \quad |p_4| = \frac{1}{R_z C_I} > \frac{g_{mI}}{C_C} = GBW$$

Zero Cancellation (cont'd)

$$R_z = \frac{(C_C + C_{II})}{g_{mII} C_C} \approx \frac{(C_{II})}{g_{mII} C_C}$$

$$C_{II} \gg Cc$$

$$\frac{1}{R_z C_I} > \frac{g_{mI}}{C_C} = GBW$$

substituting Rz

$$\frac{g_{mII} C_C}{C_I C_{II}} > \frac{g_{mI}}{C_C}$$

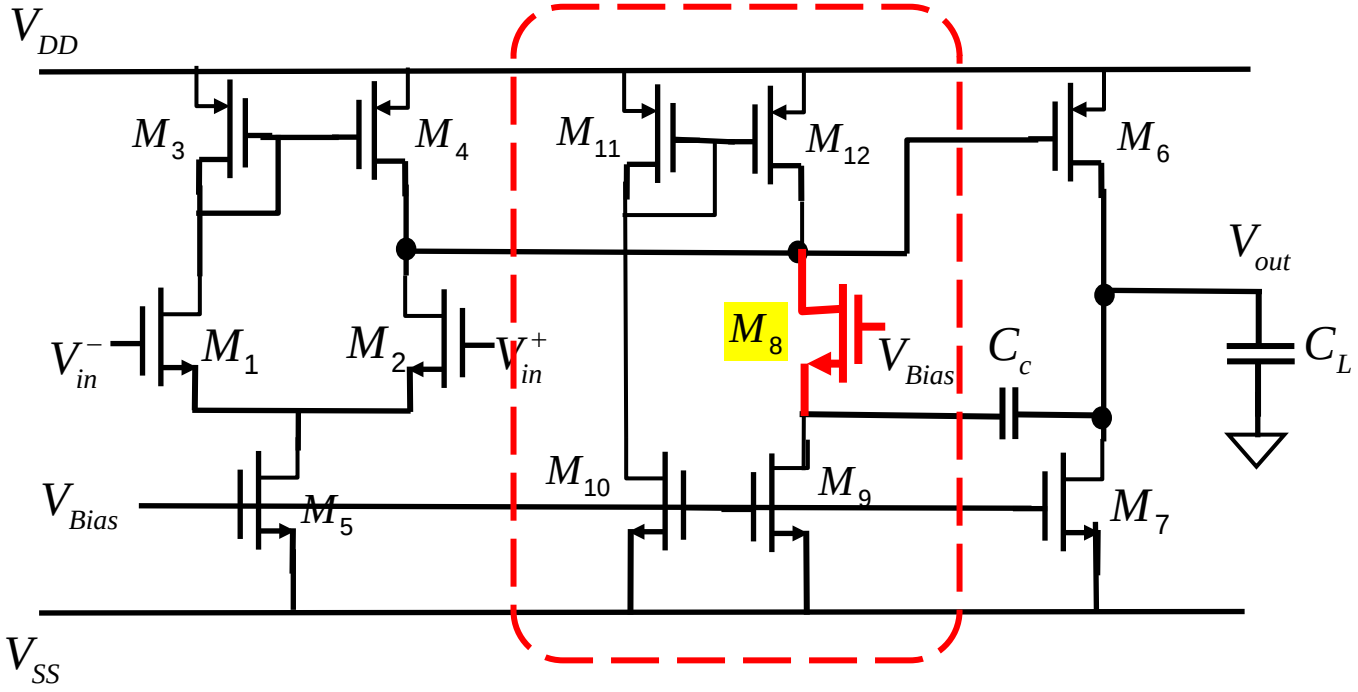
This procedure gives **excellent stability** for a fixed value of C2 (≈ CL).

Unfortunately, as **CL changes**, so does p2. Hnce, the zero must be **adjusted** to cancel p2.

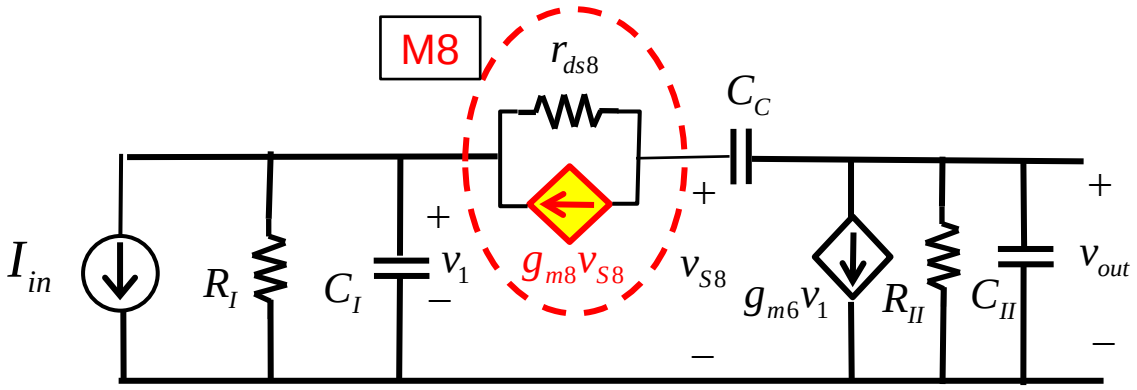
$$C_C > \sqrt{\frac{g_{mI}}{g_{mII}} C_I C_{II}}$$

Pushing p2 Farther

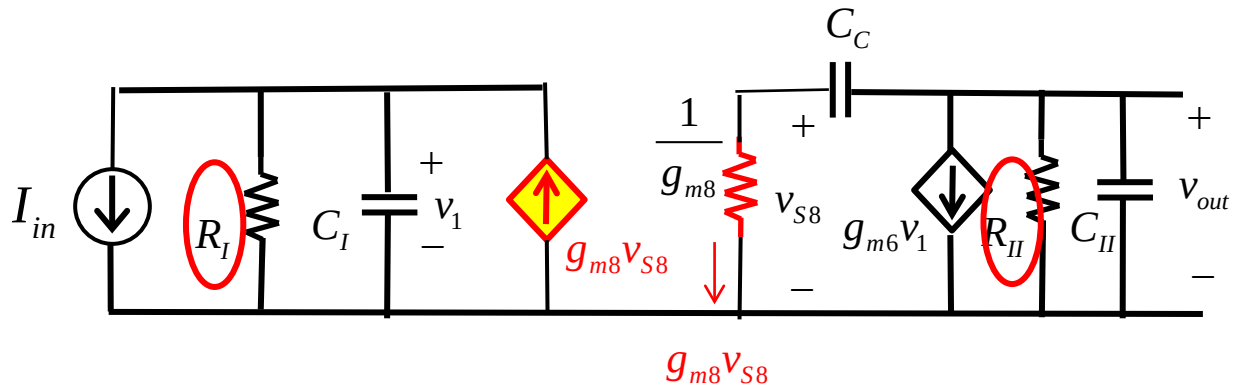
The magnitude of the **output pole (p2)** can be increased by **introducing gain in the feedback path of Miller capacitor (Cc)**.



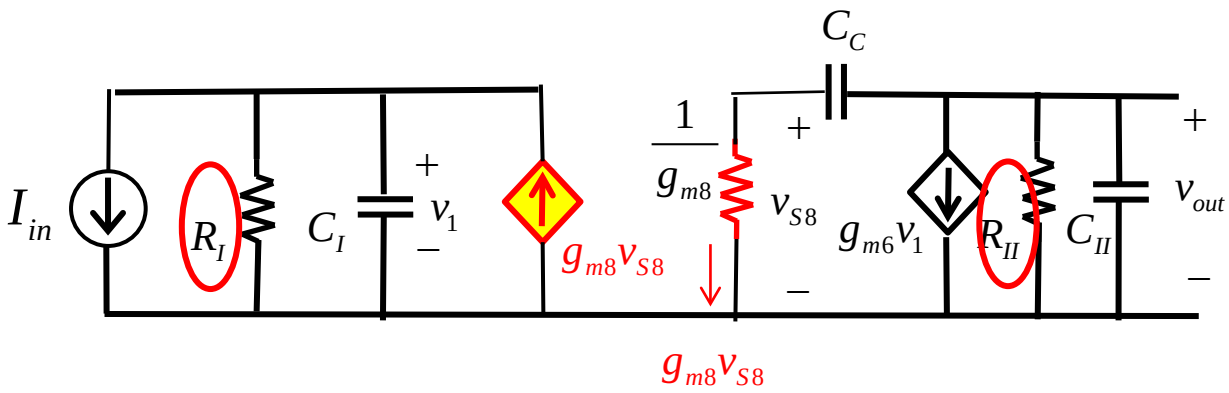
Small-Signal Model



(equiv.) $r_{ds8} = 0$



(cont'd)



The resistors R_I and R_{II} are defined as

$$R_I = \frac{1}{g_{ds2} + g_{ds4} + g_{ds12}} \approx \frac{1}{3g_{ds}} = \frac{r_{ds}}{3};$$

$$R_{II} = \frac{1}{g_{ds6} + g_{ds7}} \approx \frac{1}{2g_{ds}}$$

Assuming all the channel resistances are equal to r_{ds}.

Small-Signal Analysis

LHP zero

$$\frac{V_{out}}{I_{in}} = \left(\frac{-g_{m6}}{G_I G_{II}}\right) \frac{\left(1+\frac{sC_C}{g_{m8}}\right)}{1+s\left(\frac{C_C}{g_{m8}}+\frac{C_{II}}{G_{II}}+\frac{C_C}{G_{II}}+\frac{g_{m6}C_C}{G_I G_{II}}\right)+s^2\left(\frac{C_C C_{II}}{g_{m8}G_{II}}\right)}$$

(Derived by DPI)

$$\frac{1}{p_1 p_2}$$

⇨ **Poles are**

$$p_1 = \frac{-1}{\frac{C_C}{g_{m8}}+\frac{C_C}{G_{II}}+\frac{C_{II}}{G_{II}}+\frac{g_{m6}C_C}{G_I G_{II}}} \approx \frac{-6}{g_{m6}r_{ds}^2 C_C}$$

$$G_I = 3r_{ds}^{-1}, G_{II} = 2r_{ds}^{-1}$$

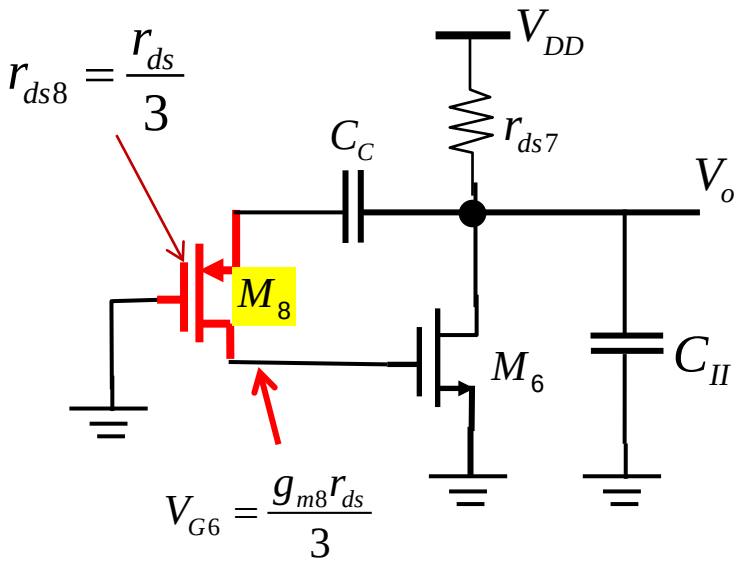
p1 is roughly unchanged while the output pole has been multiplied by ($g_m r_{ds}/3$).

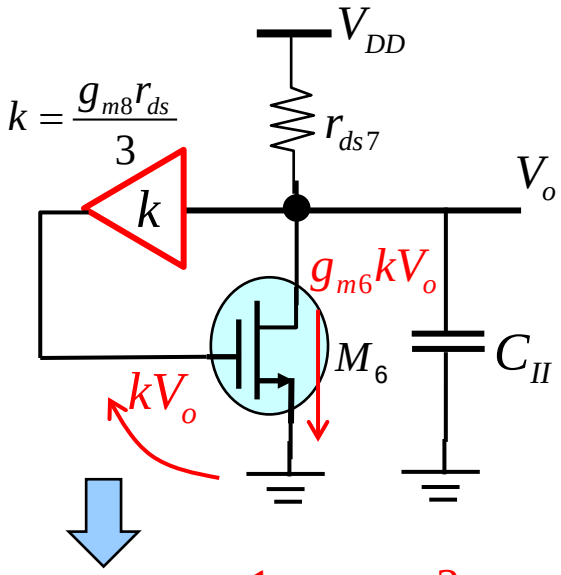
$$p_2 \approx \frac{-g_{m6}r_{ds}^2 C_C}{6\frac{C_C C_{II}}{g_{m8}G_{II}}} = -\frac{g_{m8}r_{ds}^2 G_{II} g_{m6}}{6C_{II}} = -\frac{1}{3}g_{m8}r_{ds}\left|p_2'\right|$$

$$p_2' = -\frac{g_{mII}}{C_{II}} = -\frac{g_{m6}}{C_{II}}$$

p2' is the output pole of the regular Miller compensation

Conceptual Interpretation





Output impedance of M6 is reduced

$$R_{out,M6} \approx \frac{1}{k g_{m6}} = \frac{3}{g_{m6} g_{m8} r_{ds}}$$

$$R_{out} \approx r_{ds7} \parallel \frac{3}{g_{m6} g_{m8} r_{ds8}} \approx \frac{3}{g_{m6} g_{m8} r_{ds8}}$$

$$|p_2| \approx \frac{g_{m6} g_{m8} r_{ds}}{3 C_{II}}$$ **(output pole)**

Remark: The **common gate M_8** stops the feedforward path, **preventing the occurrence of an RHP zero**.

$$z = -\frac{g_{m8}}{C_C}$$

Design Attempt (Assignment 3)

- **Please attempt to modify the circuit structure of the 2-stage Miller-compensated opamp using the techniques learned in this lecture.**
- **You may attempt to use one or two techniques introduced in this lecture.**
- **Describe your attempts clearly in your turn-in.**
- **Most likely your new design will fail ...**
- **Then try to analyze why your new design fails, what are the main reasons you guess?**
- **In case you have observed improvement; try to analyze why and how such improvement is achieved.**
- **Feel free to use the AICE tool.**
- **You are allowed to form 2~3 students as a working group by submitting one report.**

References

- P. E. Allen's lecture, ECE 6412, Analog Integrated Circuit Design –II, Georgia Tech, 2002.
- B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," IEEE J. of Solid-State Circuits, vol. SC-18, no. 6, Dec. 1983, pp. 629-633.
- G. Palmisano and G. Paumbo, "A compensation strategy for two-stage CMOS opamps based on current buffer," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 44, no. 3, pp. 257–262, Mar. 1997.*
- J. Mahattanakul and J. Chutichatuporn, "Design procedure for two-stage CMOS opamp with flexible noise-power balancing scheme," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol. 52, no. 8, pp.* 1508–1514, Aug. 2005.
- J. Mahattanakul, "Design procedure for two-stage CMOS operational amplifiers employing current buffer," IEEE Trans. on CAS – II: Express Briefs, vol. 52, no. 11, Nov. 2005.