Lecture 6
Opamp Sizing
(Part 1: Traditional Method)

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2015

Outline

- Performance targets
- Sizing targets
- Opamp design procedure
  - Empirical procedure for manual sizing
- Techniques for enhancing GBW
  - Nulling resistor
  - Voltage buffer
  - Current buffer
- Sizing with voltage/current buffers

Reference Paper

- **This lecture was mainly based on the following paper:**

- **G. Palmisano, G. Palumbo, and S. Pennisi, "Design procedure for two-stage CMOS transconductance operational amplifiers: a tutorial," Analog Integrated Circuits and Signal Processing, vol. 27, pp. 179-189, 2001.**

Motivation

- **Transistor sizing is one of the most difficult design stages to automate ;**
- **Sizing involves large / highly non-linear design space.**
- **So far, No fully automatic analog sizing tools are available for used either in industry or classroom.**

- **With manual design, design space exploration in the transistor weak and moderate inversion regions becomes even harder.**

List of Performance Targets

- **Noise**
- **Phase margin (PM or M_ϕ)**
  - **If (M_ϕ) is not given, then minimize the settling time.**
- **Gain-Bandwidth Product (GBW)**
- **Load capacitance (C_L)**
- **Slew rate (SR)**
- **Input Offset Voltage**
- **Input Common Mode Range (CMR)**
- **Output Swing (OS)**
- **Common Mode Rejection Ratio (CMRR)**
- **Power Supply Rejection Ration (PSRR)**

} **Not optimized during the manual design stage**

Comments on CMRR/PSRR

- **Design parameters such as dc gain, CMRR and PSRR**
  - **depend on the MOS output resistance (rds);**
  - **They are not easily modeled for hand analysis.**

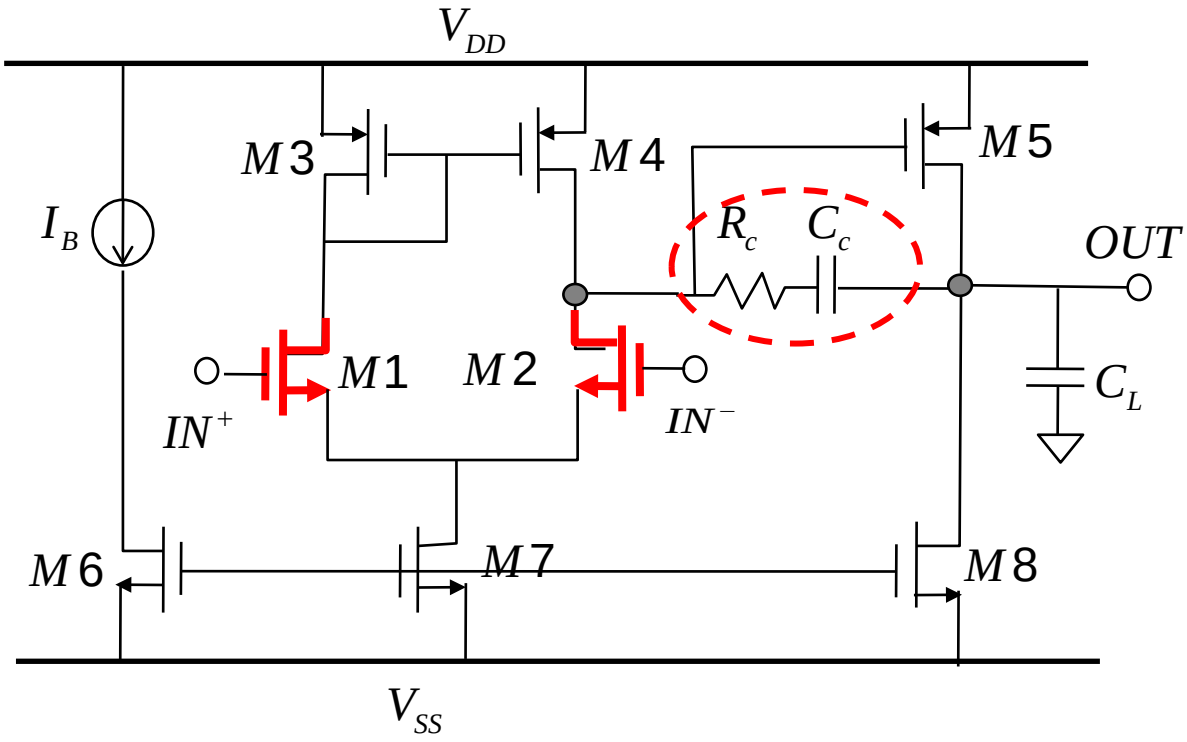
- **These parameters highly depend on the amplifier topology.**
  - **For a two-stage opamp, typical dc gain in the range of 60-80dB (1,000x to 10,000x).**
  - **CMRR in the rage of 70-90dB.**
  - **They are predicted mainly by SPICE simulation using accurate transistor models.**

Sizing Targets

- **Biasing current**
- **Inversion levels**
- **Aspect ratios (W/L) of all transistors**
- **Compensation resistor (Rc) / capacitor (Cc)**

Palmisano, Palumbo and Pennisi (2001).

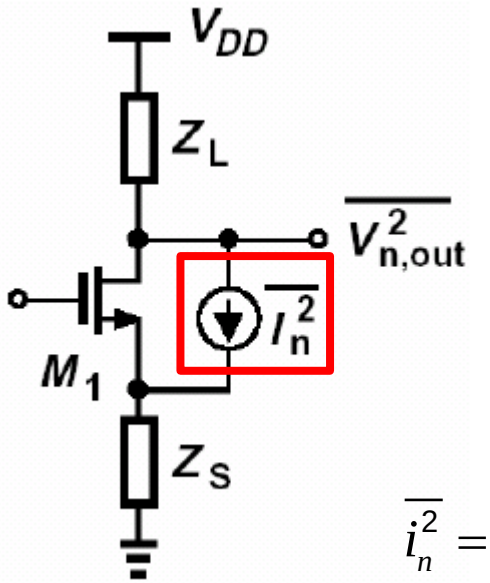
Two-stage Opamp



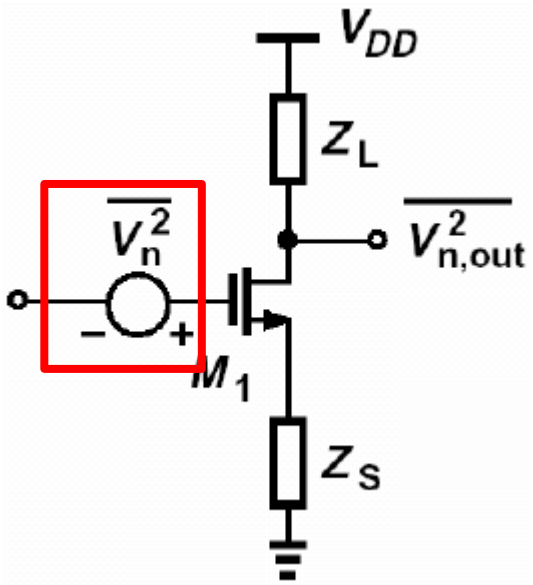
Two-stage opamp (nMOS input)

Our working circuit in this course (2015)

Noise in Transistor



$$\overline{i_n^2} = 4kT\frac{2}{3}g_m\Delta f$$



Useful Lemma: The given two circuits are equivalent if $\overline{V_n^2} = \overline{I_n^2}/g_m^2$

Noise of Input Stage

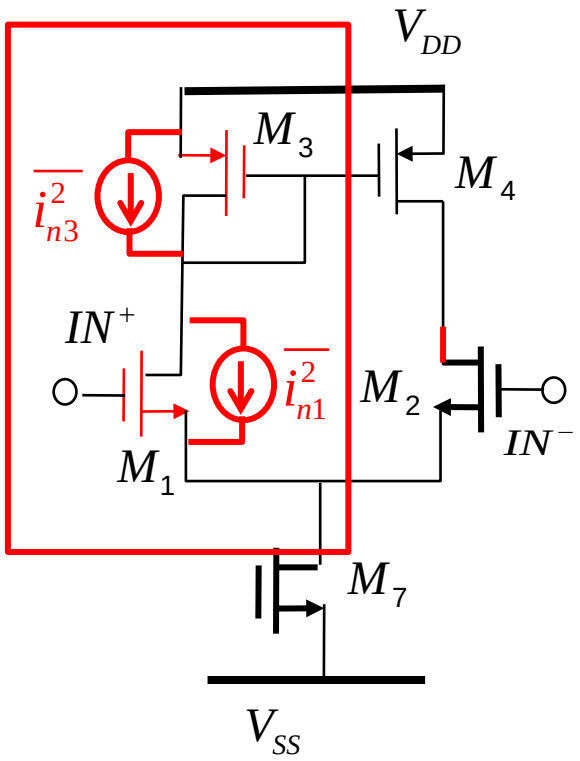
Input referred noises (@ gate of M1):

1) Due to M3:

$$\overline{i_{n3}^2} = 4kT\frac{2}{3}g_{m3} \Rightarrow \overline{v_{n1\leftarrow 3}^2} = \frac{\overline{i_{n3}^2}}{g_{m1}^2} = 4kT\frac{2}{3}\frac{g_{m3}}{g_{m1}^2}$$

2) Due to M1:

$$\overline{i_{n1}^2} = 4kT\frac{2}{3}g_{m1} \Rightarrow \overline{v_{n1}^2} = \frac{\overline{i_{n1}^2}}{g_{m1}^2} = 4kT\frac{2}{3}\frac{1}{g_{m1}}$$



Total IRN (two branches, doubled):

$$S_n(f) = \boxed{2}\times 4kT\frac{2}{3}\frac{1}{g_{m1,2}}\left(1+\frac{g_{m3,4}}{g_{m1,2}}\right)$$

Design Procedure (by Palmisano et al.)

Step 1) Start from the noise requirement.

Neglecting the flicker noise at low frequency, the **input noise voltage spectral density** is given by

$$S_n(f) = 2 \times 4kT \frac{2}{3} \frac{1}{g_{m1,2}} \left(1 + \frac{g_{m3,4}}{g_{m1,2}} \right) \qquad (1)$$

To minimize noise, we assume (by sizing) $g_{m3,4} \ll g_{m1,2}$ **so that (1) is approximated by**

$$g_{m1,2} \approx \frac{16}{3} \frac{kT}{S_n(f)} \qquad \left(g_{m3,4} \ll g_{m1,2} \right) \Rightarrow$$

So, noise spec determines $g_{m1,2}$

The low frequency flicker noise can be lowered by increasing L and W of M1 and M2 (the input pair).

Compensation Capacitor (Cc)

Step 2) The **compensation capacitor (Cc)** is determined by **$g_{m1,2}$ and the GBW requirement**:

$$\omega_T = \frac{g_{m1,2}}{C_C} \quad \Rightarrow \quad \boxed{C_C = \frac{g_{m1,2}}{\omega_T} = \frac{g_{m1,2}}{2\pi f_T}}$$

Slew Rate

- **Step 3) The slew rate depends on two part:**
- **-- the slew at the output node of the 1st stage (internal slew rate)**
- **-- and slew at the output node of the 2nd stage (external slew rate).**

The slew rates are related to the quiescent currents $I_{D1,2}$ (input stage) and I_{D8} (output stage) :

$$SR_{\text{int}} = \frac{2I_{D1,2}}{C_C} = \frac{I_{D7}}{C_C}; \quad \text{(internal)}$$

$$SR_{ext} = \frac{I_{D8} - I_{D7}}{C_L} \quad \text{(external)}$$

In practice, we would set both internal and external SR's ≥ target SR.
However, at the beginning let us set: $SR_{int} = SR_{ext} = SR$.

SR (cont'd)

(external)

$$SR = \frac{I_{D8} - I_{D7}}{C_L}$$

(internal)

$$SR = \frac{2I_{D1,2}}{C_C} = \frac{I_{D7}}{C_C};$$

$$I_{D7} = C_C SR$$

$$C_L SR = I_{D8} - C_C SR$$

$$SR = \frac{I_{D8}}{C_C + C_L}$$

$$I_{D8} = SR\left(C_C + C_L\right) = \frac{\left(C_C + C_L\right)}{C_C} I_{D7}$$

which determines the current ratio between I_{D8} & I_{D7}.

Sizing M1,2

Step 4) Size the input transistors.

$$I_D = \frac{\beta}{2}\left[2(V_{GS} - V_T) - V_{DS}\right]V_{DS};$$

$$\beta = \mu C_{ox}\frac{W}{L} = K_{n,p}\frac{W}{L}$$

$$I_{DSAT} = \frac{\beta}{2}(V_{GS} - V_T)^2 = \frac{\beta}{2}(V_{DSAT})^2$$

$$K_{n,p} = \mu C_{ox}$$

$$g_m = \frac{\partial V_{DSAT}}{\partial I_{DSAT}} = \beta V_{DSAT} = \sqrt{2\beta I_{DSAT}} = \sqrt{2K_{n,p}\frac{W}{L}I_{DSAT}}$$

Use this gm equation for sizing

$$\frac{W}{L} = \frac{g_m^2}{2K_{n,p}I_{DSAT}}$$

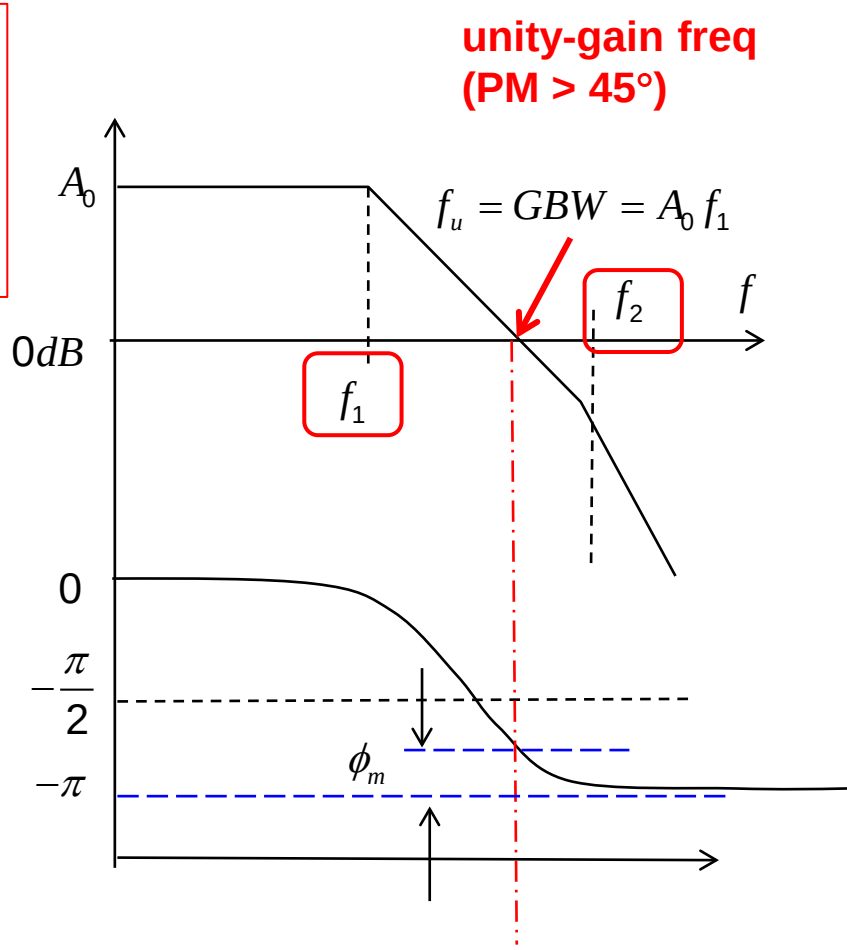
g_m and I_D determine the size ratio

Recall that gm1,2 was determined by the noise spec.

Phase Margin

Step 5) Determine the phase margin.

- **For 2-stage amplifier, the first two poles, p_1 and p_2 can approximately characterize the frequency behavior.**



Two-pole approximation of the open-loop H(s):

$$H(s) = \frac{A}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)}$$

$$\Rightarrow \quad H(j f_u) = \frac{A}{\left(1+\frac{jf_u}{f_1}\right)\left(1+\frac{jf_u}{f_2}\right)}$$

Phase Margin (cont'd)

For PM > 45°, we may approximate f_u = GBW.

$$\measuredangle H(j\omega_u) = -\tan^{-1}\frac{f_u}{f_1} - \tan^{-1}\frac{f_u}{f_2}$$

$$= -\tan^{-1}\frac{f_1 \cdot A_0}{f_1} - \tan^{-1}\frac{f_u}{f_2} \approx -\frac{\pi}{2} - \tan^{-1}\frac{f_u}{f_2}$$

(gain A_0 >> 1)

$\approx \pi / 2$

$$\measuredangle H(j\omega_u) \approx -\frac{\pi}{2} - \tan^{-1}\frac{f_u}{f_2}$$

GBW & p2 determine the PM

Phase margin: $\phi_m = \measuredangle H(j\omega_u) - (-\pi)$

$$\phi_m = \pi + \measuredangle H(j\omega_u) \approx \frac{\pi}{2} - \tan^{-1}\frac{f_u}{f_2}$$

2nd pole

Phase Margin and Poles

The phase margin (PM) is given by:

$$\phi_m = \frac{\pi}{2} - \arctan\frac{GBW}{f_2}$$

f_2: **2nd pole**

$$f_u = GBW$$

$$p_i = -2\pi f_i$$

$$\Leftrightarrow \quad \tan\phi_m = \frac{f_2}{GBW} \triangleq \chi$$

(called "separation factor" introduced by Palmisano & Palumbo 1998)

The 2nd pole occurs at: $2\pi f_2 = \frac{g_{m5}}{C_L}$

$$\Rightarrow \quad g_{m5} = 2\pi f_2 C_L = 2\pi C_L (GBW)\tan\phi_m$$

Size M5 by GBW & PM

Step 6) Determine gm5, then the size of M5.

G. Palmisano and G. Palumbo, "A novel representation for two-pole feedback amplifiers," IEEE **Trans. on Education**, vol. 41, no. 3, Aug. 1998, pp. 216-218.

Compensation Capacitor (Cc)

The "separation factor" χ:

$$\chi \triangleq \tan\phi_m = \frac{f_2}{GBW} = \frac{f_2}{f_u}$$ **(holds for PM > 45°)**

Recall the 2nd pole & GBW: $f_2 = \frac{g_{m5}}{2\pi C_L}$, $f_u = \frac{g_{m1,2}}{2\pi C_C}$

$$\Rightarrow \quad \chi = \frac{f_2}{f_u} = \frac{g_{m5}}{g_{m1,2}}\frac{C_C}{C_L}$$

$$\Rightarrow \quad \boxed{C_C = \chi \frac{g_{m1,2}}{g_{m5}} C_L}$$

Use the separation factor to determine Cc

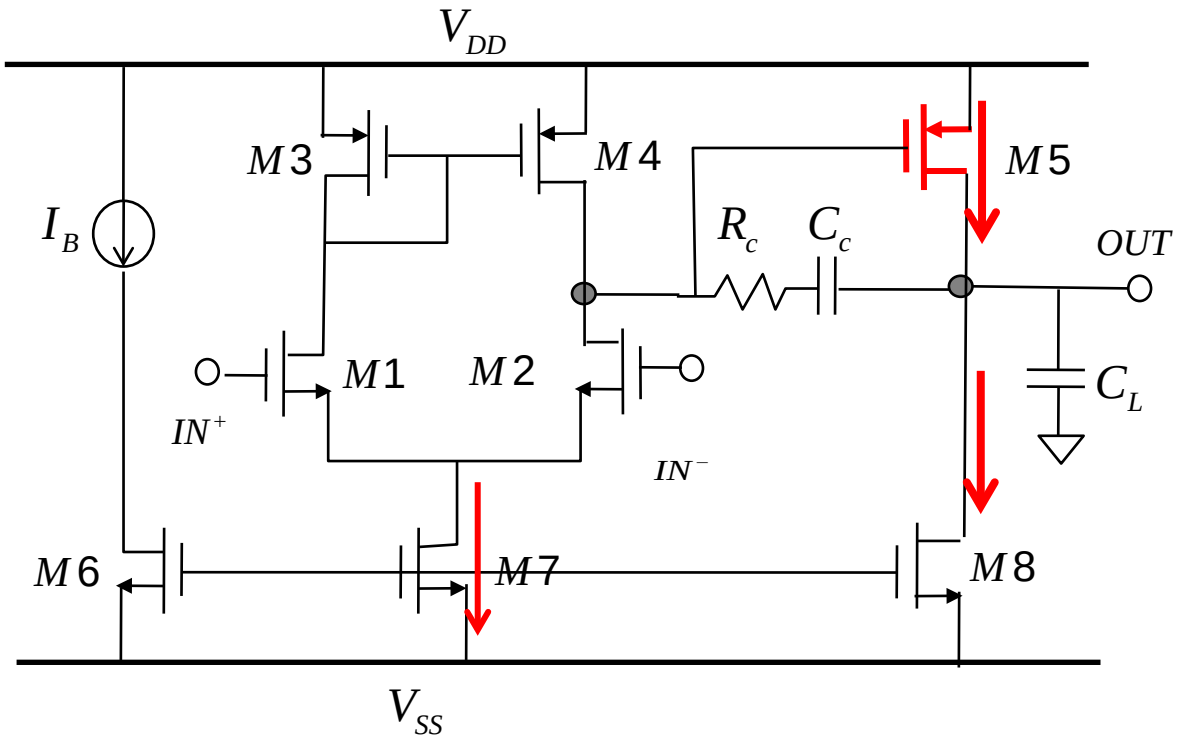
Step 7): Choose a separation factor χ (say, 2) to determine Cc.

Sizing M5

Since $I_{D5} = I_{D8}$, the size of M5 is given by

$$\left(\frac{W}{L}\right)_5 = \frac{g_{m5}^2}{2KI_{D5}}$$

I_{D7} & I_{D8} were determined by SR (step 3).



Design for Better Bandwidth

With the previous method, the maximum achievable GBW is limited by the 2nd pole $p_2 = -g_{m5}/C_L$, which depends on the load capacitor CL.

To achieve a higher GBW, a very high g_{m5} is required.

Optimize GBW with minimum change of the remaining electrical parameters.

Nulling Resistor

The left half-plane (LHP) zero introduced by the nulling resistor Rc is

$$f_Z = \frac{1}{2\pi}\frac{g_{m5}}{(1-g_{m5}R_C)C_C}$$

Setting $R_c = 1/g_{m5}$ pushes the RHP zero to infinity.

Further increasing Rc flips over the zero into LHP.

Pole-zero Cancellation

$$f_z = \frac{1}{2\pi}\frac{g_{m5}}{(1-g_{m5}R_z)C_z} = f_2 = -\frac{g_{m5}}{2\pi C_L} \qquad (1)$$

We shall determine C_z and R_z .

Insertion of the nulling resistor (R_C) results in the new (3rd) pole:

$$f_3^{new} = \frac{1}{2\pi R_z C_I}, \qquad C_I = C_{db2} + C_{db4} + C_{gs5}$$

Cap load of 1st stage

Again, define the new separation factor

$$\chi = \frac{f_3^{new}}{f_{GBW}} = \frac{C_C}{g_{m1,2}R_C C_I} \qquad (2)$$

f_3^{new}

Pole-Zero Cancellation (cont'd)

Zero cancels the old 2nd pole:

(zero) $$\frac{g_{m5}}{(g_{m5}R_C - 1)C_Z} = \frac{g_{m5}}{C_L};$$ (old 2nd pole)

$$\chi = \frac{C_Z}{g_{m1,2}R_Z C_I}$$ separation with p3(new)

$$C_L = g_{m5}R_C C_Z - C_Z$$

$$R_Z = \frac{C_Z}{\chi g_{m1,2} C_I};$$

$$\Rightarrow \quad \frac{g_{m5}}{\chi g_{m1,2} C_I} C_Z^2 - C_Z - C_L = 0$$

(Using a different notation for Cc)

Use eqns (1) & (2) to solve Cz:

$$\Rightarrow \quad C_Z = \frac{\chi g_{m1,2} C_I \left(1 + \sqrt{1 + \frac{4 g_{m5} C_L}{\chi g_{m1,2} C_I}}\right)}{2 g_{m5}} \approx \sqrt{\frac{\chi g_{m1,2} C_I C_L}{g_{m5}}}$$

$$R_Z = \sqrt{\frac{C_L}{\chi g_{m1,2} g_{m5} C_I}};$$

Cc derived earlier without Rz (assume same χ)

$$\sim C_C = \chi \frac{g_{m1,2}}{g_{m5}} C_L$$

Nulling Resistor (cont'd)

The compensation capacitor (with R) is named Cz ;
that without R is named Cc .
If choosing Cz < Cc, we might be able to achieve higher GBW.

$$C_Z = \sqrt{\frac{\chi g_{m1,2} C_I C_L}{g_{m5}}} \quad \leq \quad C_C = \chi \frac{g_{m1,2}}{g_{m5}} C_L$$

$$GBW = \omega_T = \frac{g_{m1,2}}{C_C}$$

$$C_I \leq \chi \frac{g_{m1,2}}{g_{m5}} C_L$$

Or

$$\chi \geq \frac{g_{m5}/C_L}{g_{m1,2}/C_I}$$

$f_z = p_2$

f_T of the 1st stage with nulling resistor

$$GBW = \omega_T = \frac{g_{m1,2}}{C_Z}$$

Now (Cz is reduced!)

Choosing this separation factor will help achieve a higher GBW.

Sizing with compensation for Eliminating the RHP Zero

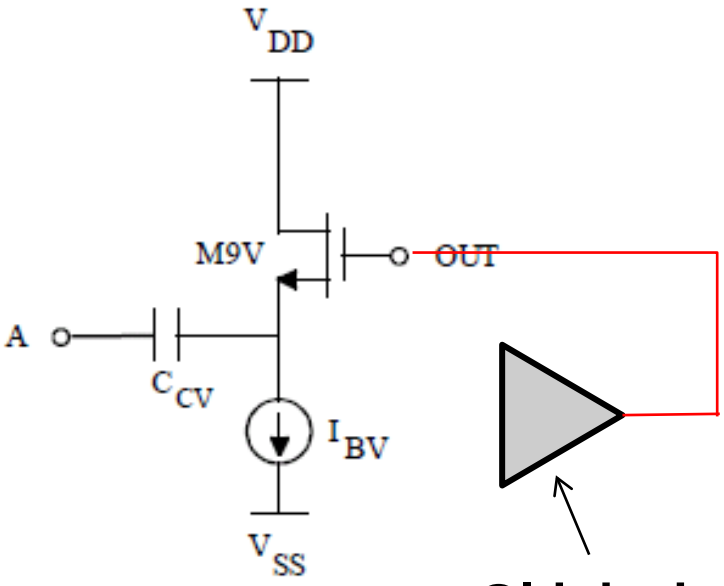
Voltage buffer compensation & current buffer compensation.

Closed-loop Stability

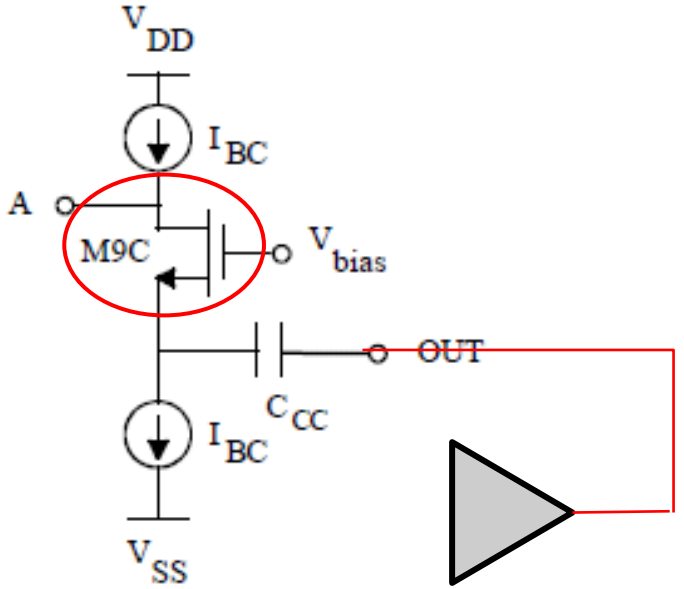
- **For two-stage opamps, adding the Miller capacitor Cc results in the pole-splitting phenomenon which improves the closed-loop stability significantly.**
- **However, the Miller capacitor also creates a feed-forward path which leads to a RHP zero.**
- **Such a zero can be relocated by connecting a series nulling resistor, or**
- **Connecting a common-gate current buffer (**Mahattanakul, 2005), **etc.**

J. Mahattanakul, “Design procedure for two-stage CMOS operational amplifiers employing current buffer,” IEEE Trans. CAS-II: Express Briefs, vol. 52, no. 11, Nov. 2005, pp. 766-770.

Voltage/Current Buffer Compensation



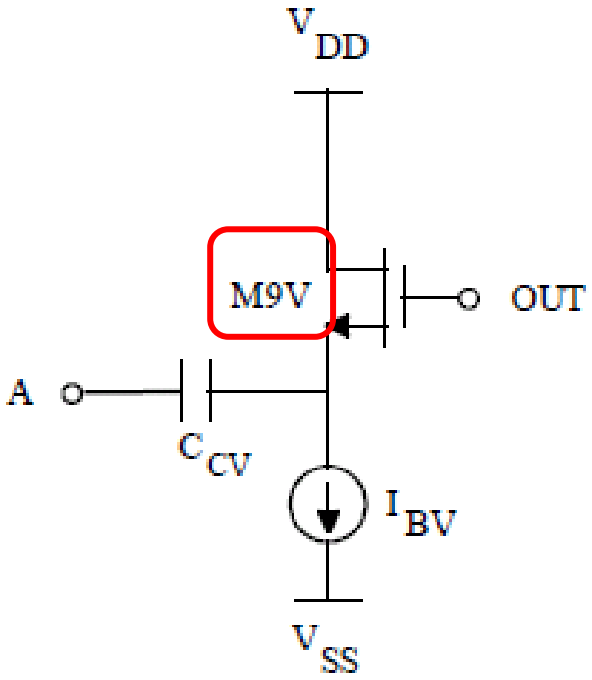
Old design



Modification by adding voltage buffer (VB)

Modification by adding current buffer (CB)

Sizing with Voltage Buffer



VB breaks the compensation path into indirect connection, eliminating a possible zero path.

The buffer transistor M9 has an output resistance $1/g_{o,9}$.

The compensation path introduces a LHP zero at

$$f_z = -\frac{g_{o,M9}}{2\pi C_{CV}}$$

cf. the prev lecture

We may let this zero cancel the 2nd pole:

$$\frac{g_{m5}}{C_L} = \frac{g_{o,M9}}{C_{CV}}$$

Cancelling the 2nd pole (cont'd)

$$\frac{g_{m5}}{C_L} = \frac{g_{o,M9}}{C_{CV}} \quad (1)$$

This equation has two unknowns: $g_{o,M9}$ and C_{CV}.

Second, we derive the new 2nd pole after inserting the VB:

$$f_2^{new} = \frac{g_{o,M9}}{2\pi C_{eq}}$$

$$C_{eq} = C_I + C_{gs9V} \approx C_I$$

C_I is the 1st stage output capacitance

Now new GBW becomes

$$f_{GBW}^{new} = \frac{g_{m1,2}}{C_{CV}}$$

New separation factor

$$\chi = \frac{f_2^{new}}{f_{GBW}^{new}} = \frac{g_{o,M9} C_{CV}}{g_{m1,2} C_{eq}} \quad (2)$$

VB (cont'd)

Use equations (1), (2) to solve:

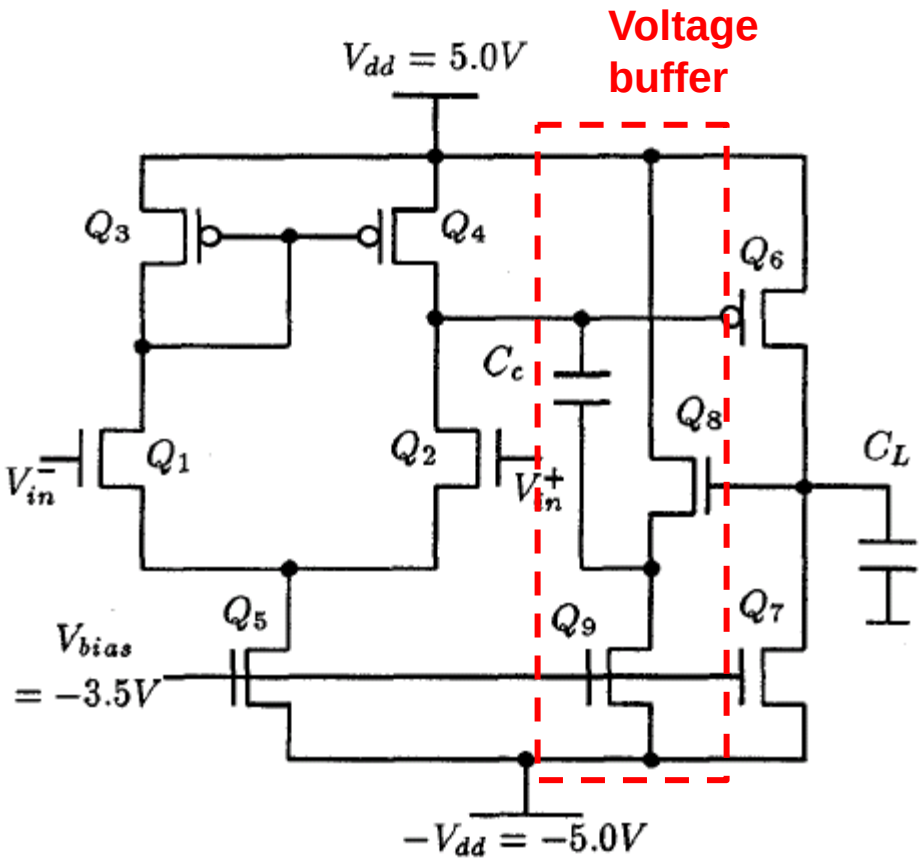
$$\begin{cases} \dfrac{g_{m5}}{C_L} = \dfrac{g_{o,M9}}{C_{CV}}; \\ \chi = \dfrac{g_{o,M9} C_{CV}}{g_{m1,2} C_{eq}} \approx \dfrac{g_{o,M9} C_{CV}}{g_{m1,2} C_I} \end{cases}$$

$$\Rightarrow \quad \begin{cases} g_{o,M9} \approx \sqrt{\chi g_{m5} g_{m1,2} \dfrac{C_I}{C_L}} \\ C_{CV} \approx \sqrt{\chi C_I C_L \dfrac{g_{m1,2}}{g_{m5}}} \end{cases} \quad \leftarrow$$

Ccv approximately equals to Cz derived before for nulling resistor compensation

Another paper that presents sizing for VB compensation

Sizing with VB Compensation



Two-stage with voltage buffer (VB) compensation

The stage of Q8-Q9 provides voltage buffer compensation

P. Mandal and V. Sisvanathan, "Macromodeling of the AC characteristics of CMOS op-amps," Proc. IEEE/ACM ICCAD, pp. 334-340, **1993**.

Design Equations

Sizing all transistors into saturation ...

Assume that the body effect parameters (λ_i's) and the bias voltages are independent of the transistor widths.

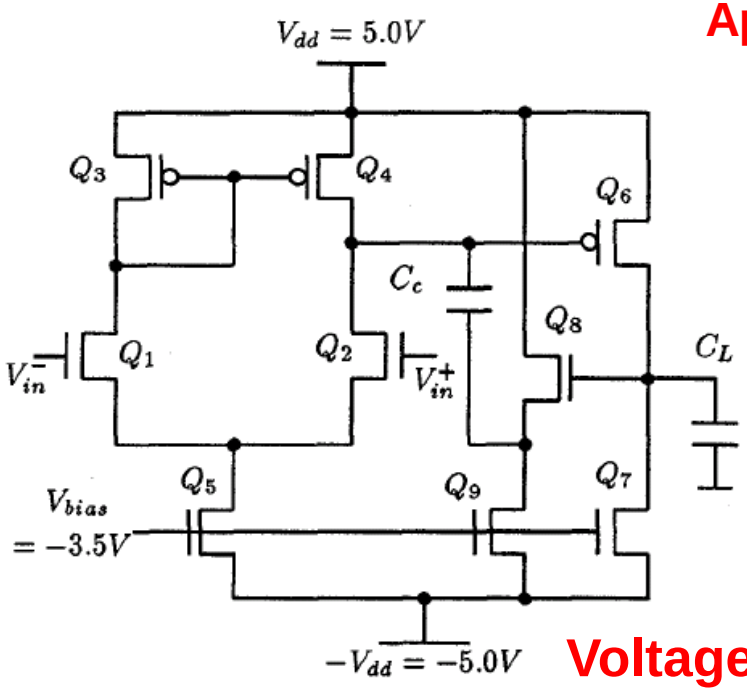
DC gain:

$$A_0 \approx \frac{g_{m1} g_{m6}}{(g_{ds1} + g_{ds3})(g_{ds6} + g_{ds7})} \approx K \sqrt{\frac{W_1 W_6}{W_5 W_7}}$$

$$K = \mu C_{ox}$$

The output resistances of gds3, gds6 are proportional to the drain currents of M5 & M7, respectively.

DC Gains (more details)



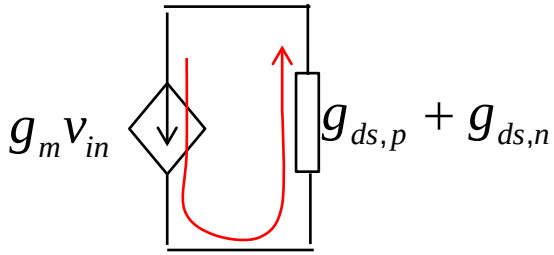
Approximate dc gain:

$$A_0 \approx \left[\frac{g_{m1}}{(g_{ds1} + g_{ds3})}\right]\left[\frac{g_{m6}}{(g_{ds6} + g_{ds7})}\right] \approx K\sqrt{\frac{W_1 W_6}{W_5 W_7}}$$

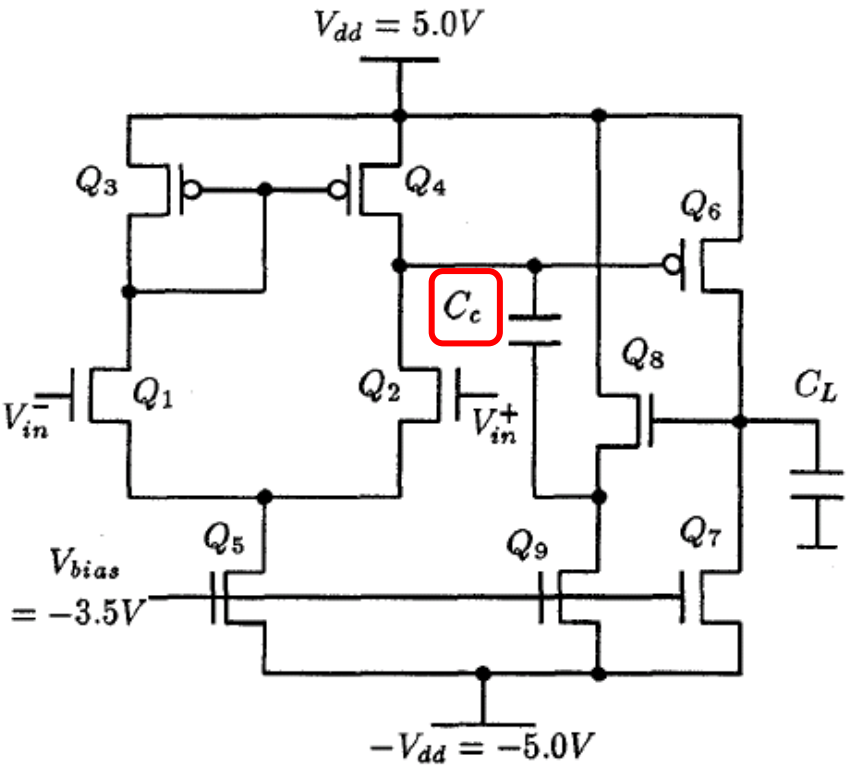
gain of 1st stage:

gain of 2nd stage:

Voltage buffer



Dominant Pole



The first pole is

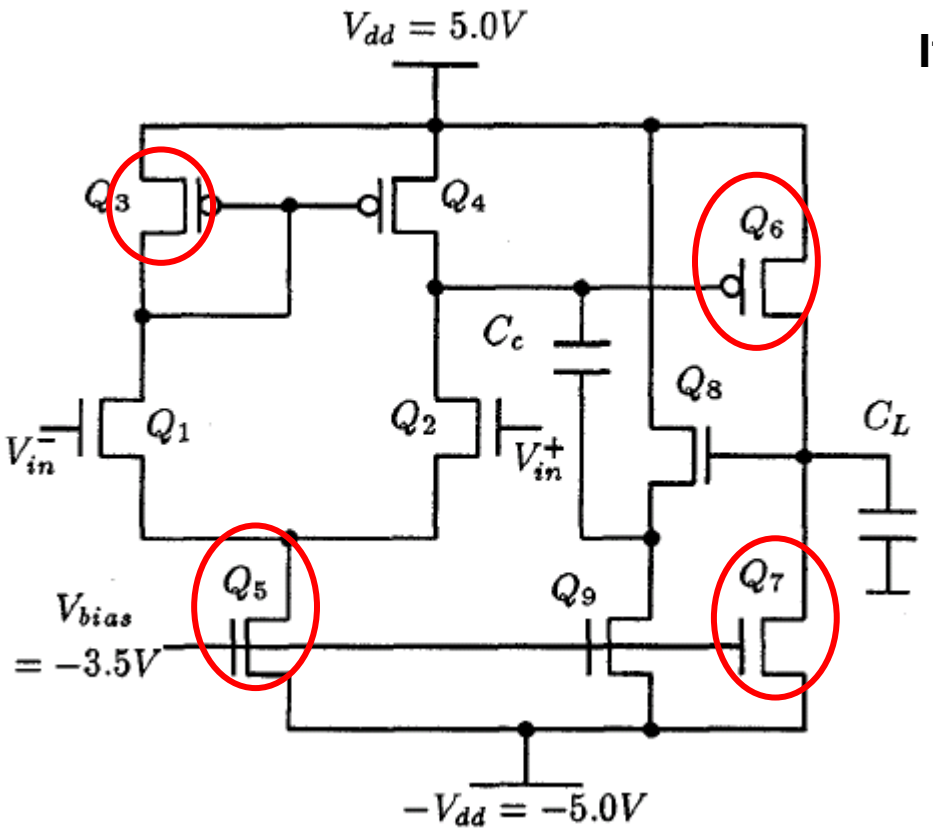
$$p_1 \approx \frac{(g_{ds1} + g_{ds3})(g_{ds6} + g_{ds7})}{C_C g_{m6}} \approx K \frac{W_5}{C_C} \sqrt{\frac{W_7}{W_6}}$$

$$p_1 \approx \frac{(g_{ds1} + g_{ds3})(g_{ds6} + g_{ds7})}{C_C g_{m6}} = \frac{1}{R_I (C_C g_{m6} R_{II})}$$

(R_I: $g_{ds1} + g_{ds3}$; R_{II}: $g_{ds6} + g_{ds7}$)

Miller effect Cc

Sizing



The $I_{D,3}$ is half $I_{D,5}$; and the drain currents of $I_{D,6}$ = $I_{D,7}$ are equal.

It follows that:

$$\frac{\left(\frac{W}{L}\right)_3 (1-\lambda_p V_{ds,3})}{\left(\frac{W}{L}\right)_6 (1-\lambda_p V_{ds,6})} = \frac{\frac{1}{2}\left(\frac{W}{L}\right)_5 (1+\lambda_n V_{ds,5})}{\left(\frac{W}{L}\right)_7 (1+\lambda_n V_{ds,7})}$$

Assume:

$$(1-\lambda_p V_{ds,3}) = (1+\lambda_n V_{ds,5})$$

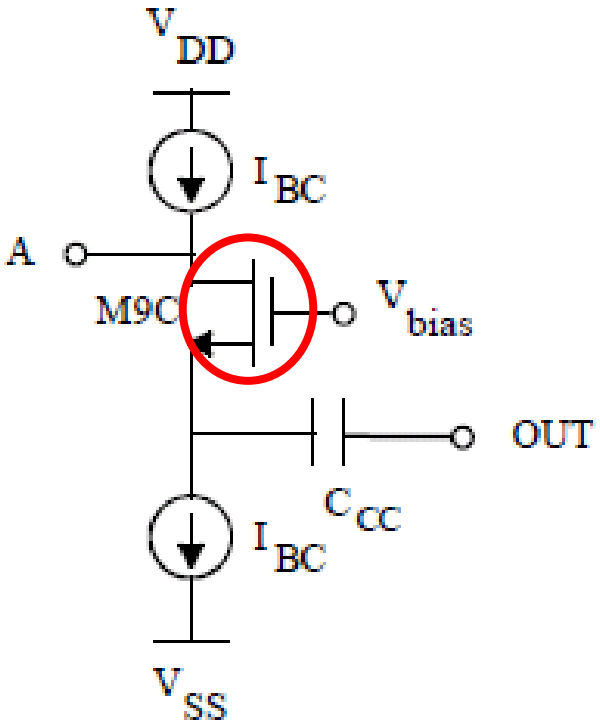
$$\lambda_p \approx \lambda_n$$

$$-V_{ds,6} = V_{ds,7}$$

$$\Rightarrow \quad \frac{W_6}{W_7} = 2\frac{W_3}{W_5}$$

Other mentioning of the literature

Sizing for Current Buffer Compensation



Current buffer

According to (Palmisano and Palumbo,1997), the optimal GBW is achieved by

$$g_{m9C} = 2g_{m1,2};$$

$$C_{CC} \approx \sqrt{\frac{g_{m1,2}}{g_{m5}}\left(\frac{2K-1}{2+K}+\frac{1}{2}\right)C_L C_I}$$

$$K = \mu C_{ox}$$

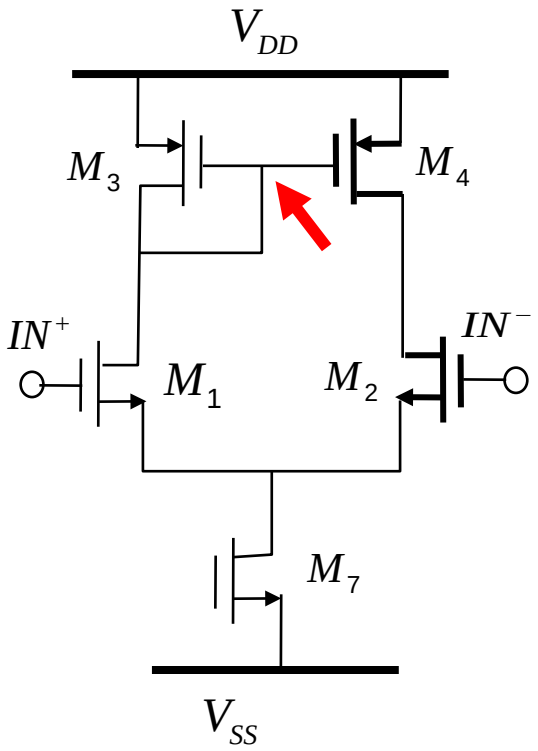
Also called common gate current buffer Miller compensation (CBMC)

G. Palmisano and G. Palumbo, “A compensation strategy for two-stage CMOS opamps based on current buffer,” IEEE Trans. on CAS-I, vol. 44, no. 3, pp. 257-262, March 1997.

Caution on Doublet

The current mirror (M3-M4) may introduce a pole-zero doublet with $s_z > 2*s_p$.

The doublet can be ignored in the traditional design, but must be considered with R_Z, VB, and CB compensations due to the higher GBW.



* The issue of doublet is discussed in another lecture.

Doublet Issue (cont'd)

The doublet-pole frequency is approximately (verify?) at

$$f_{db} \approx \frac{g_{m3,4}}{2\pi 2C_{gs4}}$$

The new GBW is approximately given by (cf. Palmisano and Palumbo, 1999**):**

$$f_{GBW}^{new} \approx \frac{2 f_2 f_{db}^2}{\chi f_{db}(f_{db} + f_2)}$$

The new compensation capacitor can be calculated by:

$$C_{C,new} \approx \frac{f_{GBW} C_C}{f_{GBW}^{new}}$$

G. Palmisano and G. Palumbo, "Analysis and compensation of two-pole amplifiers with a pole-zero doublet," IEEE Trans. on CAS-I, vol. 46, no. 7, pp. 864-868, July 1999.

Paper Reading

The following paper is recommended for reading

- **J. Mahattanakul, "Design procedure for two-stage CMOS operational amplifiers employing current buffer," IEEE Trans. CAS-II: Express Briefs, vol. 52, no. 11, Nov. 2005, pp. 766-770.**

- **containing detailed small-signal analysis and sizing info.**

References

- P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 2nd ed. Oxford University Press, Oxford, 2002.
- B. K. Ahuja, “An improved frequency compensation technique for CMOS operational amplifiers,” IEEE J. Solid-State Circuits, vol. SC-18, no. 3, pp. 629–633, Jun. 1983. (original proposal of the current buffer technique, but lacks detailed analysis)
- G. Palmisano, G. Palumbo, and S. Pennisi, “Design procedure for two-stage CMOS transconductance operational amplifiers: a tutorial,” Analog Integrated Circuits and Signal Processing, vol. 27, pp. 179-189, 2001. (introduced in this lecture)
- G. Palmisano and G. Palumbo, “A novel representation for two-pole feedback amplifiers,” IEEE Trans. on Education, vol. 41, no. 3, Aug. 1998, pp. 216-218.
- J. Huijsing, R. Hogervorst, and K. de Langen, “Low-power low-voltage VLSI operational amplifier cells,” IEEE Trans. on Cicruits and Systems – II, vol. 42, pp. 841-852, Nov. 1995.
- G. Palmisano, G. Palumbo, and R. Salerno, “CMOS output stages for low voltage power supply,” IEEE Trans. on CAS – II, vol. 47, no. 2, pp. 96-104, Feb. 2000.

Appendix