Lecture 7
Analysis of Current Amplifiers

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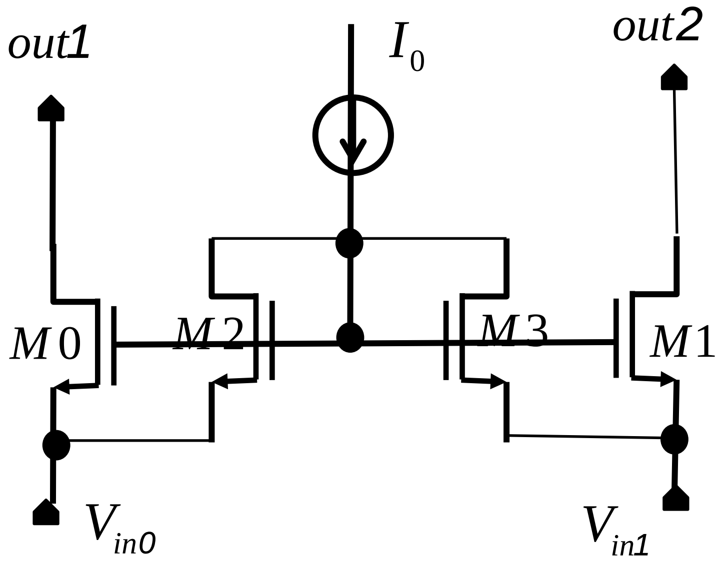
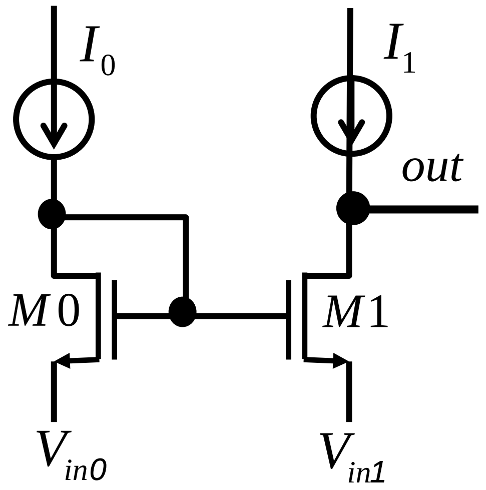
Outline

- **Symmetric current amplifier (DC, AC analysis)**
- **Asymmetric current amplifier (DC, AC analysis)**

Useful Current Amplifier Cells





Symmetric current amplifier

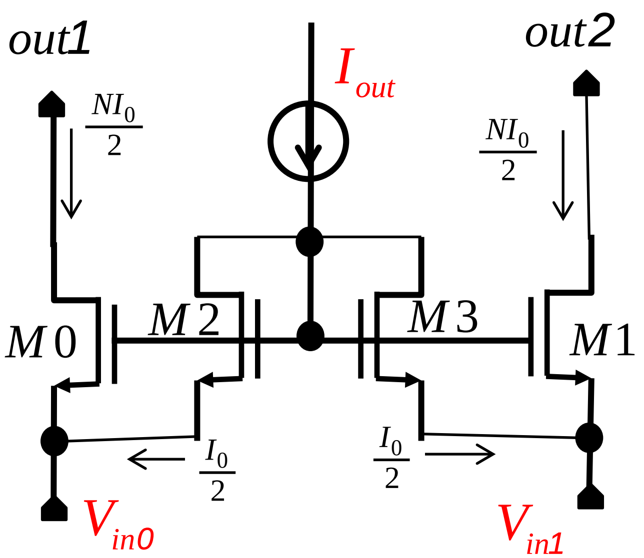
Asymmetric current amplifier

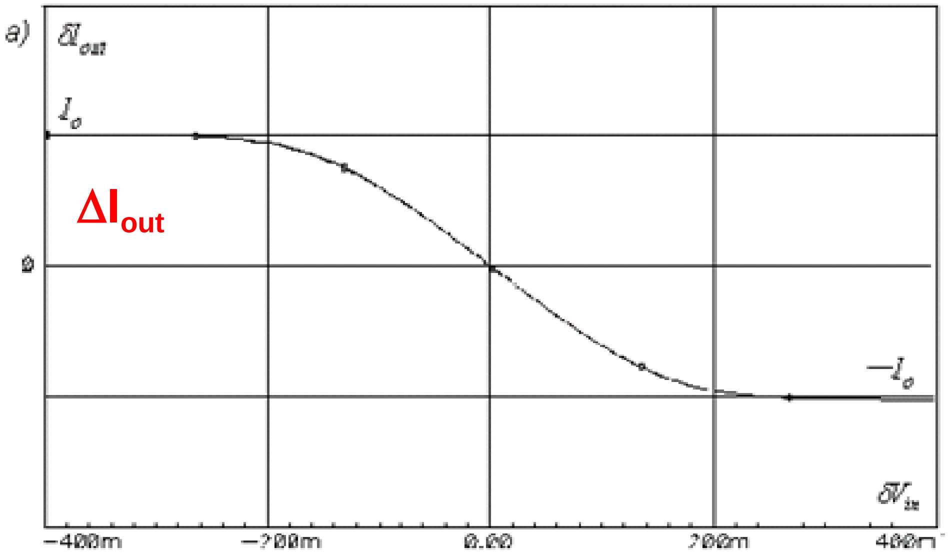
Symmetric: Detailed Analysis

I. Symmetric current amplifier (DC, AC analysis)

Symmetric Current Amplifier

$$\Delta I_{out} \equiv I_{D2} - I_{D3}$$



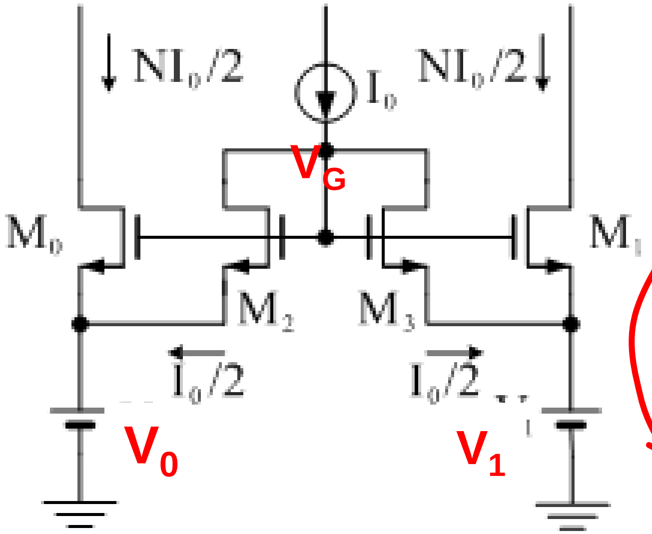


ΔV_{in}

$$\Delta V_{in} \equiv V_{in0} - V_{in1}$$

HW: Please verify this circuit using HSPICE.

DC Analysis (Math)



$$V_{GS3} = V_G - V_1; \qquad V_{GS2} = V_G - V_0;$$

$$\Delta V_{in} \equiv V_0 - V_1 = V_{GS3} - V_{GS2}$$

$$I_D = \frac{\mu_n C_{ox}(W/L)}{2}(V_{GS} - V_{TH})^2 \Rightarrow V_{GS} - V_{TH} = K\sqrt{I_D}$$

$$K = \sqrt{\frac{2}{\mu_n C_{ox}(W/L)_2}}$$

$$\begin{cases} \Delta V = K(\sqrt{I_{D3}} - \sqrt{I_{D2}}) \\ I_{D3} + I_{D2} = I_0 \end{cases}$$

$$\Delta V = K(\sqrt{I_{D3}} - \sqrt{I_{D2}}) \Rightarrow \left(\frac{\Delta V}{K}\right)^2 = \left(\sqrt{I_{D3}} - \sqrt{I_{D2}}\right)^2 = \underbrace{I_{D3} + I_{D2}}_{I_0} - 2\sqrt{I_{D2} I_{D3}}$$

(taking square)

$$\Rightarrow 2\sqrt{I_{D2} I_{D3}} = I_0 - \left(\frac{\Delta V}{K}\right)^2 \qquad I_0 = I_{D3} + I_{D2}$$

(solve)

Math (cont'd)

$$I_{D3} + I_{D2} = I_0$$

$$2\sqrt{I_{D2} I_{D3}} = I_0 - (\Delta V / K)^2$$

$$\Delta I \equiv I_{D2} - I_{D3} = \pm\sqrt{\left(I_{D2} - I_{D3}\right)^2} = \pm\sqrt{\left(I_{D2} + I_{D3}\right)^2 - 4 I_{D2} I_{D3}}$$

$$= \pm\sqrt{I_0^2 - \left[I_0 - \left(\frac{\Delta V}{K}\right)^2\right]^2} = \pm I_0 \sqrt{1 - \left\{1 - \left(\frac{\Delta V}{K\sqrt{I_0}}\right)^2\right\}^2}$$

$$\Rightarrow \quad \Delta I \equiv I_{D2} - I_{D3} = \pm I_0 \sqrt{1 - \left[1 - \left(\frac{\Delta V}{K\sqrt{I_0}}\right)^2\right]^2}$$

Next we get the limiting values ...

Math (cont'd)

$$\Delta V_{in} = K(\sqrt{I_{D3}} - \sqrt{I_{D2}})$$

$$\Delta I \equiv I_{D2} - I_{D3} = \pm I_0 \sqrt{1 - \left[1 - \left(\frac{\Delta V}{K\sqrt{I_0}}\right)^2\right]^2}$$

the left end

$$I_0 = I_{D3} + I_{D2}$$

$$\boxed{\text{If } I_{D2} = I_0; \quad I_{D3} = 0} \Rightarrow \begin{cases} \Delta V_{in} = -K\sqrt{I_0} \\ \Delta I = +I_0 \end{cases}$$

(Limiting values)

$$\boxed{\text{If } I_{D2} = 0; \quad I_{D3} = I_0} \Rightarrow \begin{cases} \Delta V_{in} = +K\sqrt{I_0} \\ \Delta I = -I_0 \end{cases}$$

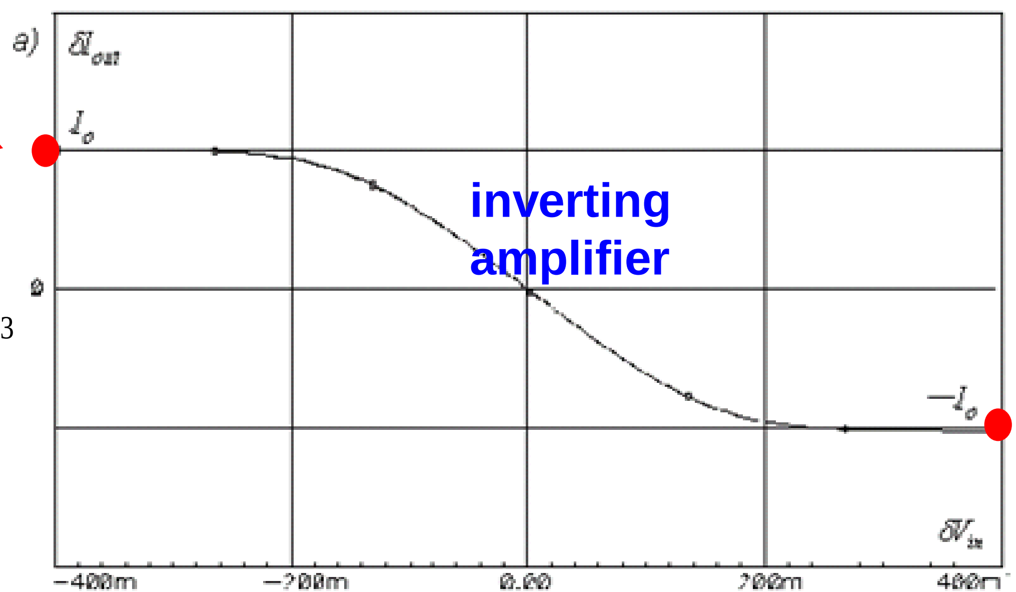
the right end

DC Characteristics

$$\begin{cases} \Delta V_{in} = -K\sqrt{I_0} \\ \Delta I_{out} = +I_0 \end{cases}$$

$$\begin{cases} \Delta V_{in} = +K\sqrt{I_0} \\ \Delta I_{out} = -I_0 \end{cases}$$

$$\Delta I_{out} \equiv I_{D2} - I_{D3}$$

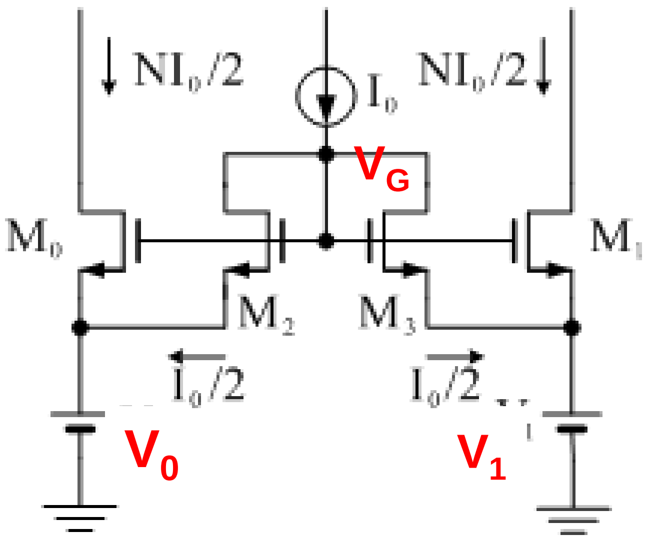


$$\Delta V_{in} = -K\sqrt{I_0}$$

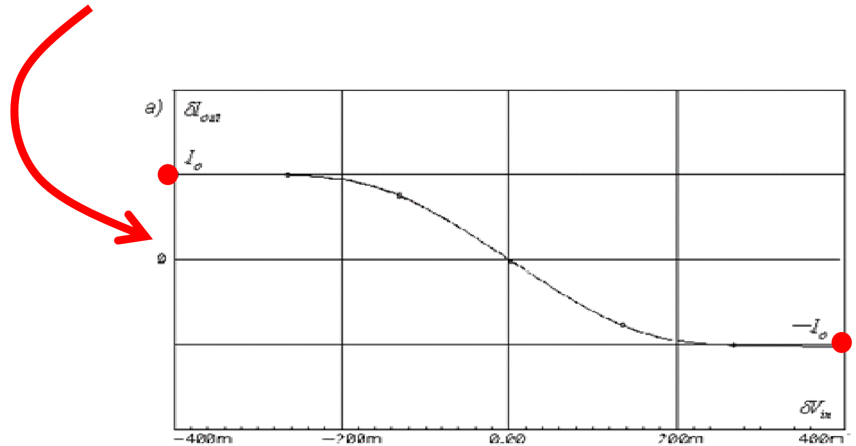
$$\Delta V_{in} := V_0 - V_1$$

$$\Delta V_{in} = +K\sqrt{I_0}$$

Symmetric Current Amplifier - Summary



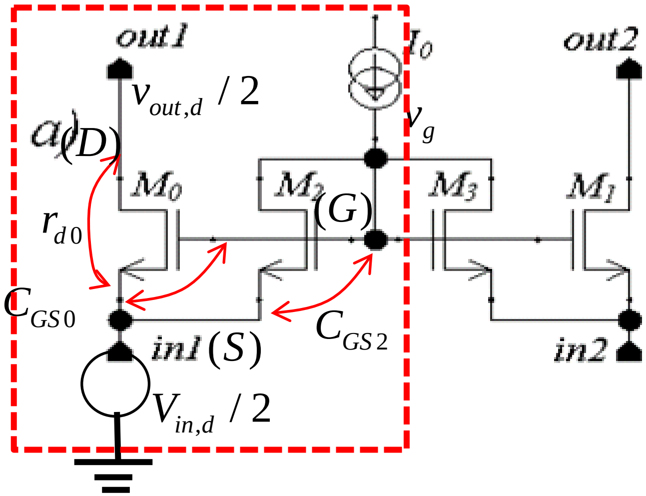
$$\Delta I_{out} \equiv I_{D2} - I_{D3}$$



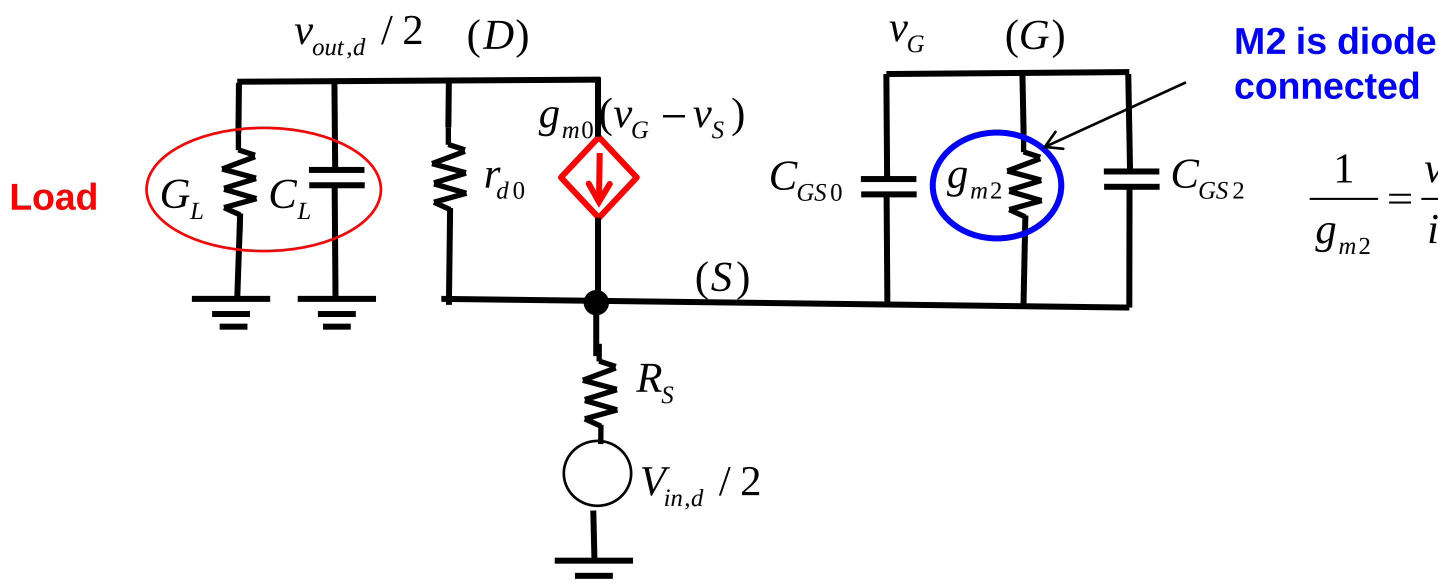
$$\Delta V_{in} \equiv V_0 - V_1$$

Positive input Δ voltage switches on the right transistor (M3) and proportionally the drain current of the right outer transistor (M1).
Negative input Δ voltage produces the opposite switching.

Symmetric: Small-signal Analysis

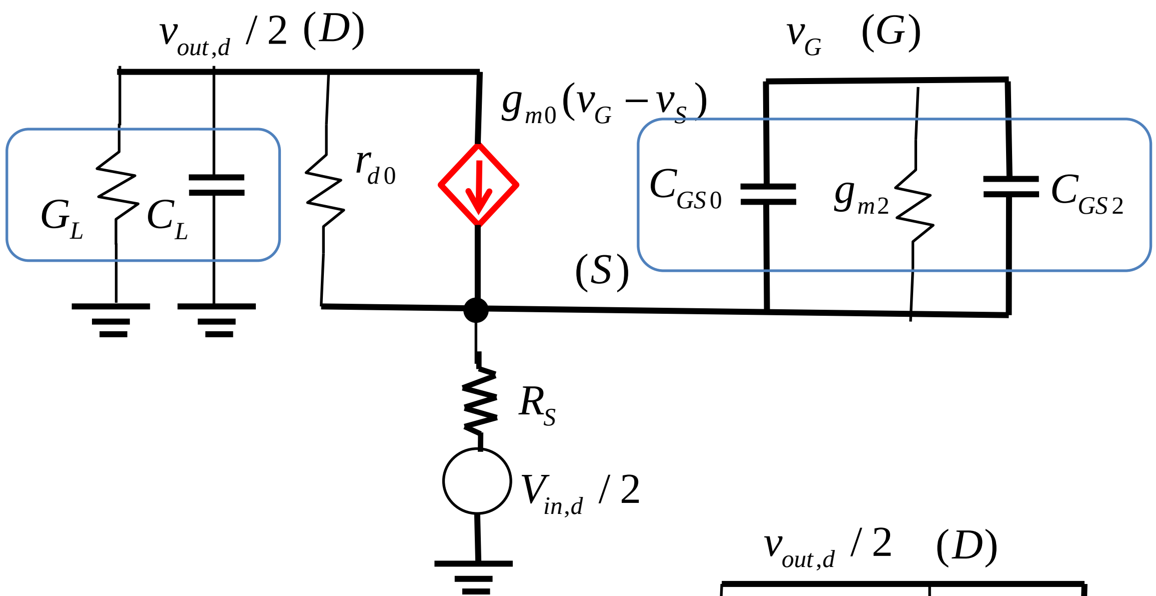


Half circuit small-signal model



$$\frac{1}{g_{m2}} = \frac{v_{GS2}}{i_{DS2}}$$

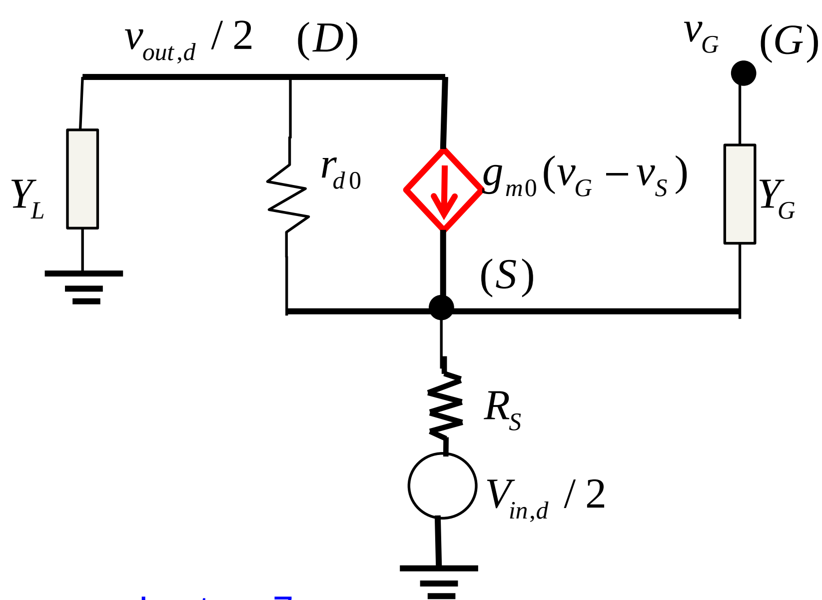
Small-signal Analysis (cont'd)



$$\frac{1}{g_{m2}} = \frac{v_{GS2}}{i_{DS2}}$$

$$Y_L := G_L + sC_L$$

$$Y_G := g_{m2} + s(C_{GS0} + C_{GS2})$$



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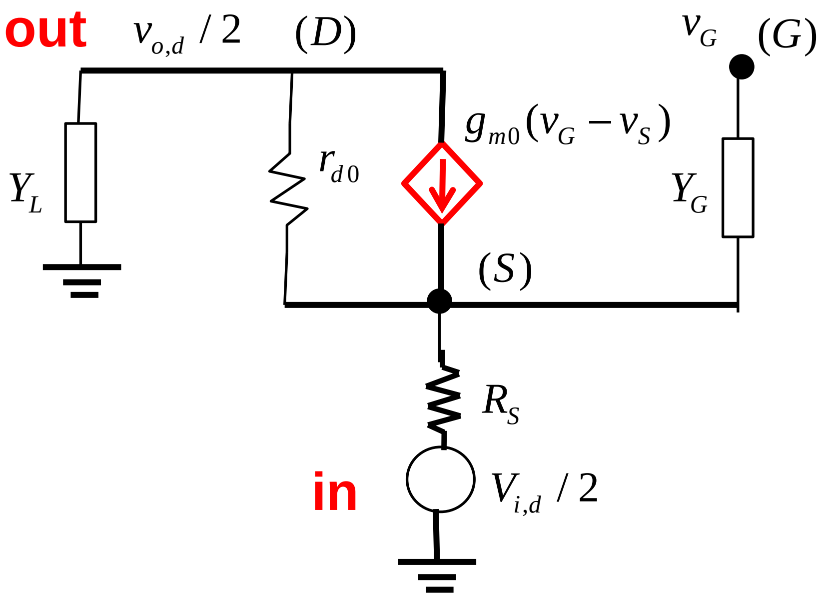


@ Drain:

$$Y_L \frac{V_{od}}{2} + \frac{1}{r_{do}}\left(\frac{V_{od}}{2} - V_S\right) + g_{mo}(V_G - V_S) = 0 \qquad \textbf{(1)}$$

@ Source:

$$-Y_L \frac{V_{od}}{2} + Y_G(V_G - V_S) = \frac{1}{R_S}\left(V_S - \frac{V_{id}}{2}\right) \qquad \textbf{(2)}$$

By (1) ➔

$$(1 + r_{do}Y_L)\frac{V_{od}}{2} + \left(1 + r_{do}g_{mo}\right)(V_G - V_S) - V_G = 0$$

By (2) ➔

$$-R_S Y_L \frac{V_{od}}{2} + (1 + R_S Y_G)(V_G - V_S) - V_G = -\frac{V_{id}}{2}$$

(cont'd)

$$(1+r_{do}Y_L)\frac{V_{od}}{2}+\left(1+r_{do}g_{mo}\right)(V_G-V_S)-V_G=0 \qquad \times(1+R_SY_G)$$

$$+ \quad -R_SY_L\frac{V_{od}}{2}+(1+R_SY_G)(V_G-V_S)-V_G=-\frac{V_{id}}{2} \qquad \times(-1)\left(1+r_{do}g_{mo}\right)$$

$$(1+R_SY_G)(1+r_{do}Y_L)\frac{V_{od}}{2}-(1+R_SY_G)V_G$$

$$+R_SY_L\left(1+r_{do}g_{mo}\right)\frac{V_{od}}{2}+\left(1+r_{do}g_{mo}\right)V_G=\left(1+r_{do}g_{mo}\right)\frac{V_{id}}{2}$$

The other half circuit will give a similar equation for V_{id}^- and V_{od}^-.

$$\left\{(1+R_SY_G)(1+r_{do}Y_L)+R_SY_L\left(1+r_{do}g_{mo}\right)\right\}\frac{V_{od}^{\pm}}{2}+(r_{do}g_{mo}-R_SY_G)V_G$$

$$=\left(1+r_{do}g_{mo}\right)\frac{V_{id}^{\pm}}{2}$$

cancelling the common-mode term

Symmetric: Small-signal analysis

$$\left\{(1+R_S Y_G)(1+r_{do}Y_L)+R_S Y_L\left(1+r_{do}g_{mo}\right)\right\}v_{od}=\left(1+r_{do}g_{mo}\right)v_{id}$$

AC gain

$$A(s)=\frac{v_{od}}{v_{id}}=\frac{1+g_{m0}r_{d0}}{[(1+Y_G r_S)r_{d0}+(1+g_{m0}r_{d0})R_S]Y_L+(1+Y_G R_S)}$$

$$A(s)=\frac{A_{ig}}{(1+Y_G R_S)(1+r_{d0}Y_L)+A_{ig}R_S Y_L}$$

$$A_{ig}=1+g_{m0}r_{d0}$$

AC (cont'd)

$$A(s) = \frac{A_{ig}}{(1+R_S Y_G)(1+r_{d0}Y_L) + A_{ig}R_S Y_L} \equiv \frac{A_{ig}}{D(s)}$$

$$Y_L := G_L + sC_L; \qquad Y_G := g_{m2} + s(C_{GS0} + C_{GS2}) = g_{m2} + sC_{GS}$$

$$C_{GS} \triangleq (C_{GS0} + C_{GS2})$$

$$D(s) \equiv (1+R_S Y_G)(1+r_{d0}Y_L) + A_{ig}R_S Y_L$$

$$A(s) = \frac{A_{ig}}{\boxed{\left\{G_L[r_{d0}(1+g_{m2}R_S) + A_{ig}R_S]\right\}}(1+\frac{s}{p_1})(1+\frac{s}{p_2})}$$

See derivation in the following pages

Approximations

$$Y_G := g_{m2} + sC_{GS}; \qquad Y_L := G_L + sC_L;$$

$$D(s) = [1 + R_S Y_G][1 + r_{d0} Y_L] + A_{ig} R_S Y_L$$

$$= [1 + R_S (g_{m2} + sC_{GS})][1 + r_{d0}(G_L + sC_L)] + A_{ig} R_S (G_L + sC_L)$$

$$= 1 + R_S (g_{m2} + sC_{GS}) + r_{d0}(G_L + sC_L)$$
$$+ R_S r_{d0}(g_{m2} + sC_{GS})(G_L + sC_L) + A_{ig} R_S (G_L + sC_L)$$

Terms of s⁰: $= \cancel{1 + R_S g_{m2}} + r_{d0} G_L + R_S r_{d0} g_{m2} G_L + A_{ig} R_S G_L$

Terms of s¹: $= \cancel{R_S C_{GS}} + r_{d0} C_L + R_S r_{d0}(g_{m2} C_L + G_L C_{GS}) + A_{ig} R_S C_L$

Terms of s²: $= R_S r_{d0} C_{GS} C_L$

Approximation (cont'd)

Terms of s⁰: $= G_L\left[r_{d0}(1+R_S g_{m2}) + A_{ig}R_S\right] = G_L B$

Terms of s¹: $= C_L\left[r_{d0}(1+R_S g_{m2}) + A_{ig}R_S\right] + R_S r_{d0} G_L C_{GS} = C_L B + R_S r_{d0} G_L C_{GS}$

Terms of s²: $= R_S r_{d0} C_{GS} C_L = E C_L$

$$B \equiv \left[r_{d0}(1+R_S g_{m2}) + A_{ig}R_S\right]$$

$$E \equiv R_S r_{d0} C_{GS}$$

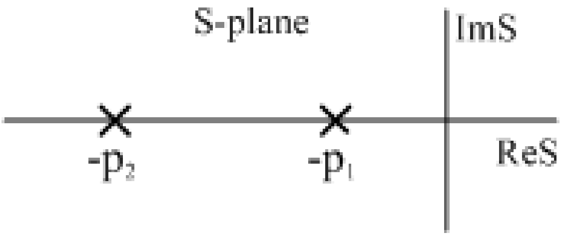
$$D(s) = G_L B + s\left(C_L B + R_S r_{d0} G_L C_{GS}\right) + s^2\left(R_S r_{d0} C_{GS} C_L\right)$$

$$= \left\{G_L B + s\left(C_L B + E G_L\right) + s^2\left(E C_L\right)\right\}$$

$$= \left\{\boxed{G_L B} + s\left(B C_L + G_L E\right) + s^2\left(E C_L\right)\right\}$$

$$= (G_L + sC_L)(B + sE) = 0$$

(cont'd)



$$D(s) = (G_L + sC_L)(B + sE) = 0$$

$$p_1 = \frac{G_L}{C_L}$$

$$A(s) = \frac{A_{ig}}{\left\{G_L[r_{d0}(1+g_{m2}R_S) + A_{ig}R_S]\right\}\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)}$$

$$p_2 = \frac{B}{E} = \frac{r_{d0}(1+g_{m2}R_S) + A_{ig}R_S}{(C_{GS0} + C_{GS2})r_{d0}R_S}$$

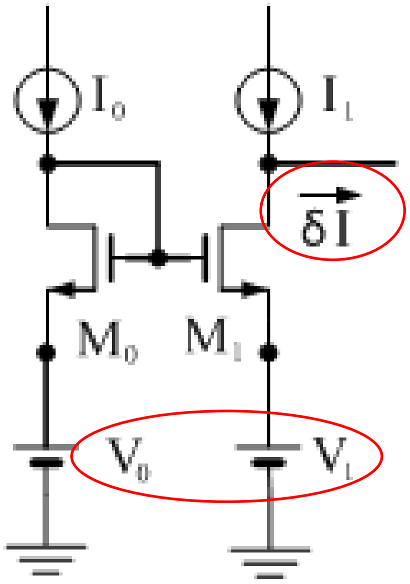
The 2nd pole is far apart from the 1st one; practically can be considered as a one-pole system defined by the load (GL // CL).

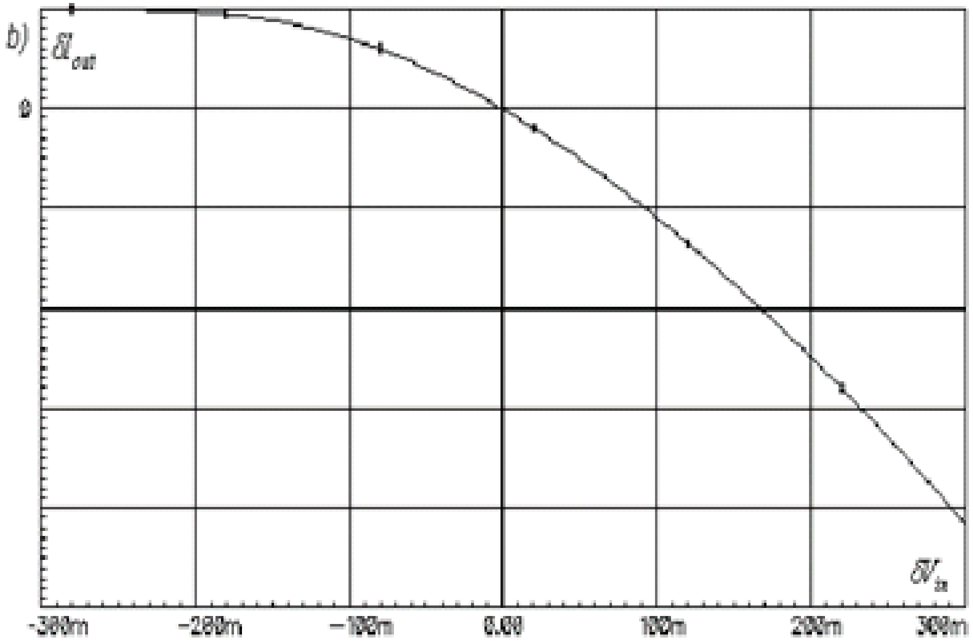
$$Y_L := G_L + sC_L; \qquad |r_{d0}Y_L| >> 1$$

Asymmetric: Detailed Analysis

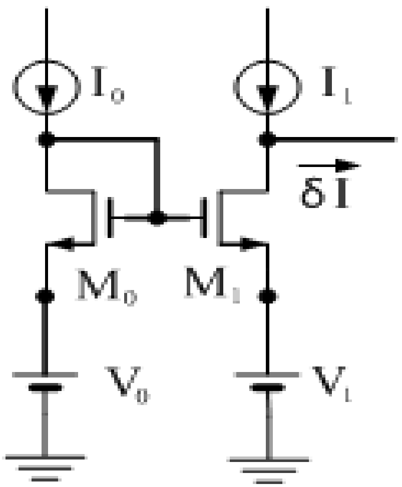
II. Asymmetric current amplifier (DC, AC analysis)

Asymmetric Current Amplifier

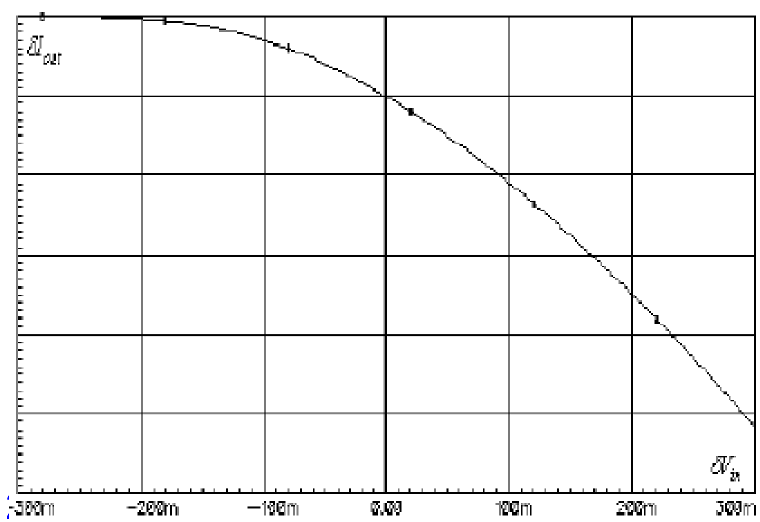




Asymmetric C.A. (DC analysis)



ΔI = f (ΔV)



$$V_0 = V_1; \quad \frac{I_1}{I_0} = \frac{(W/L)_1}{(W/L)_0}; \qquad \Delta V = V_0 - V_1$$

$$V_{eff1} \equiv V_{GS1} - V_{th} = V_G - V_1 - V_{th}$$

$$I_0 = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_0 (V_G - V_0 - V_{th})^2$$

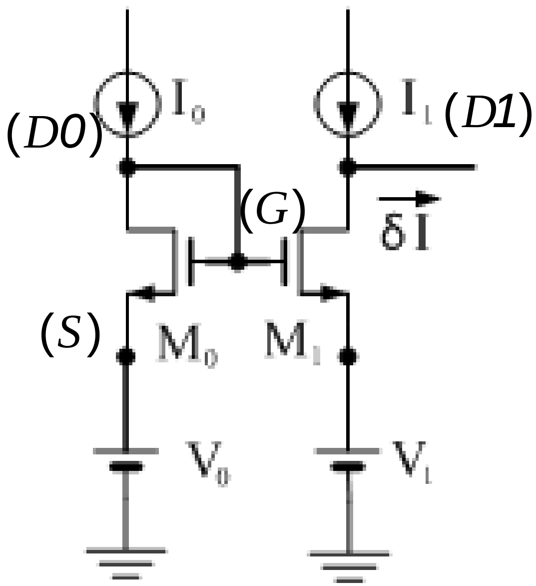
$$= \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_0 (\underbrace{V_G - V_1 - V_{th}} \underbrace{+ V_1 - V_0})^2$$

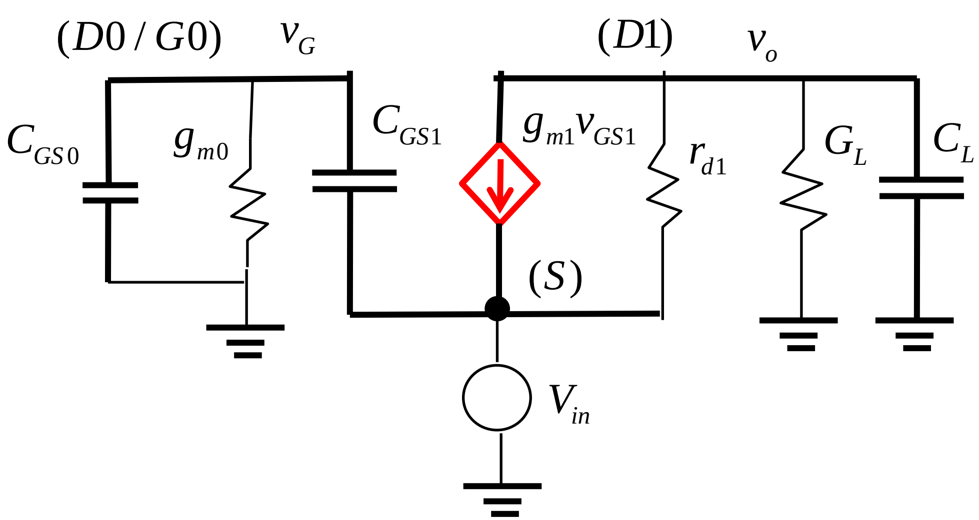
$$= \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_0 (V_{eff1} - \Delta V)^2$$

$$\Delta I = I_1 - I_0 = I_1 - \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_0 (V_{eff1} - \Delta V)^2$$

A quadratic function!

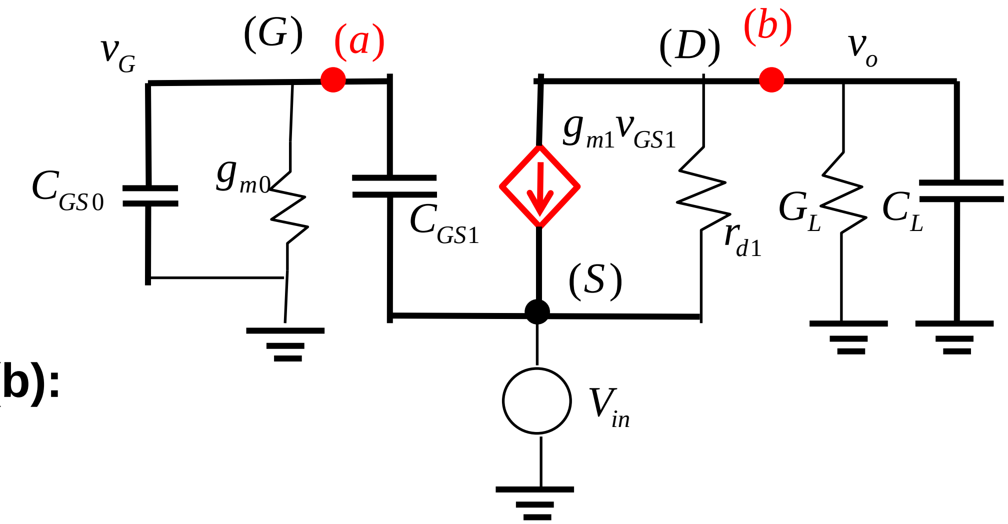
Asymmetric: Small Signal Analysis





Asymmetric: Small Signal Analysis (cont'd)

$$Y_L \equiv G_L + sC_L$$
$$Y_0 \equiv g_{m0} + sC_{GS0}$$



Write equations at nodes (a) & (b):

@ (a) $$Y_0 V_G = sC_{GS1}(V_i - V_G);$$

@ (b) $$g_{m1}(V_G - V_i) + \frac{1}{r_{d1}}(V_o - V_i) = -Y_L V_o;$$

$$\Rightarrow \quad A(s) = \frac{v_o}{v_i} = \frac{1}{(1 + r_{d1}Y_L)} \frac{(1 + g_{m1}r_{d1})Y_0 + sC_{GS1}}{(Y_0 + sC_{GS1})}$$

Asymmetric: Small-signal Analysis (cont'd)

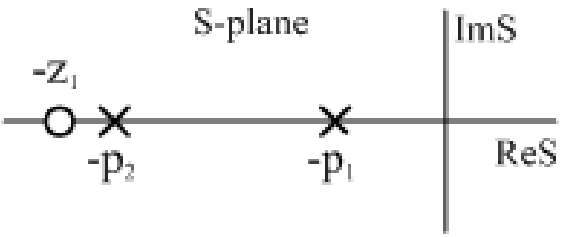
$$A(s) = A_0 \frac{(1+\frac{s}{z_1})}{(1+\frac{s}{p_1})(1+\frac{s}{p_2})}$$

$$A_0 = \frac{1+g_{m1}r_{d1}}{1+G_L r_{d1}} \approx \frac{g_{m1}}{G_L} \longleftarrow$$ **output conductance**

$$z_1 = \frac{g_{m0}}{C_{GS0} + [C_{GS1}/(1+g_{m1}r_{d1})]} \approx \frac{g_{m0}}{C_{GS0}}$$

$$p_1 = \frac{1+r_{d1}G_L}{r_{d1}C_L} \approx \frac{G_L}{C_L};$$

$$p_2 = \frac{g_{m0}}{C_{GS0}+C_{GS1}}$$

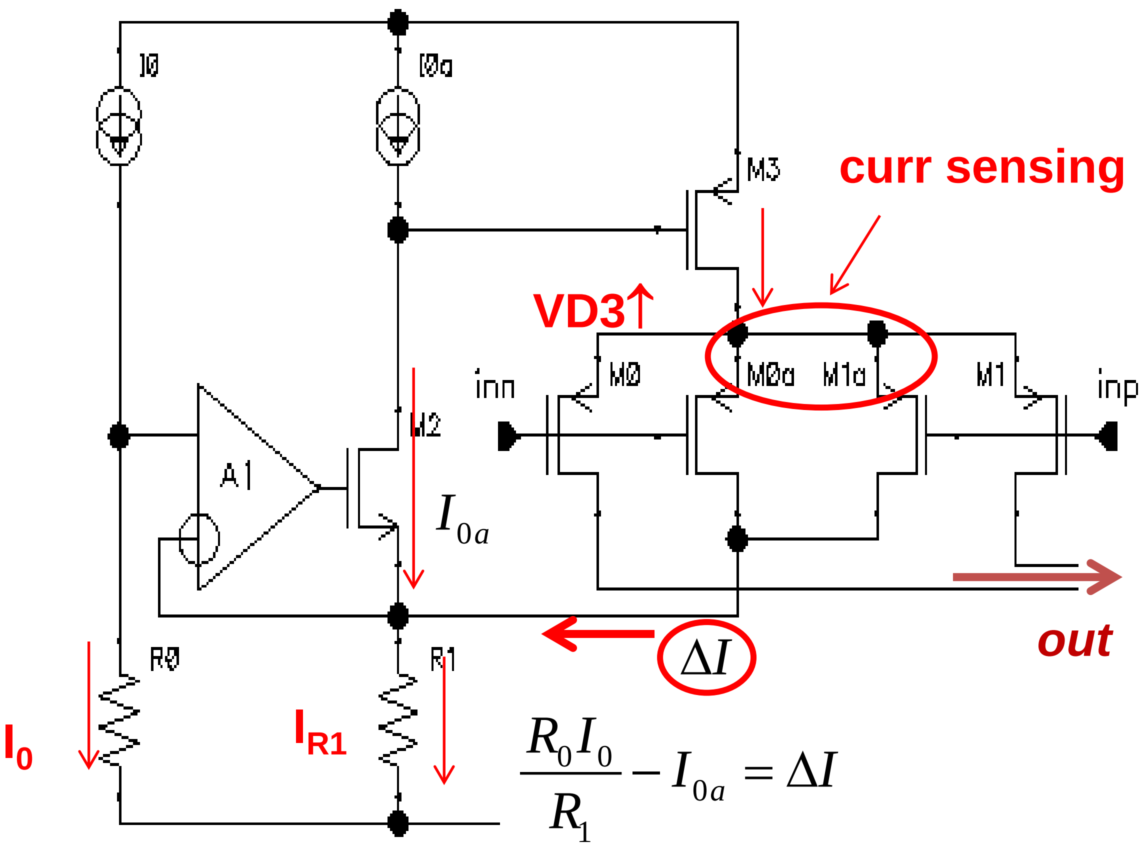


Practically one-pole system again

Designs Applying Current Amplifier

Example 1 – Current Sensing

Using symmetric current mirror



$$\frac{R_0 I_0}{R_1} - I_{0a} = \Delta I$$

$$R_0 I_0 = R_1 I_{R1}$$

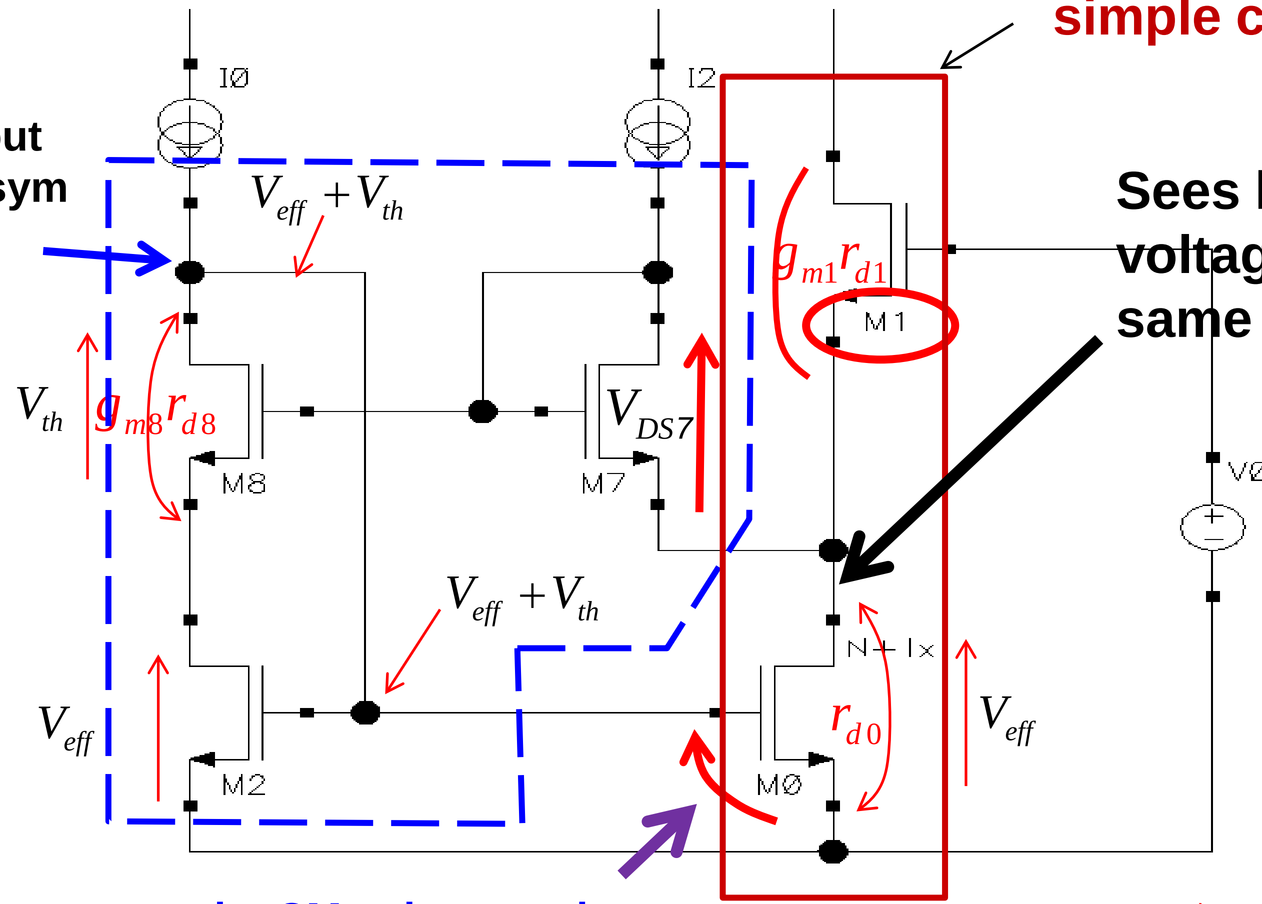
- The current arriving at the sensing transistors M0a-M1a is equal to $\Delta I = I_0(R0/R1) - I_{0a}$
- Then the current in M0 / M1 is equal to $I0 = I1 = (\Delta I/2)\ N$
- If the input voltages @ in-/in+ rise and M3 enters triode region (VD3 goes up), this relationship is still valid.

Example 2 – Enhancing output imped.

This example uses ***asymmetric current amplifier (M7-M8); NMOS configuration***

simple cascode

Output of Asym CM



Sees higher voltage given the same ID

$V_{D7} \geq V_{eff} + 2V_{th}$

$V_{DS7} \geq 2V_{th}$

➔ V_{GS} of M0 enhanced!

$r_{d0} \rightarrow r_{d0}(g_{m8} r_{d8})$

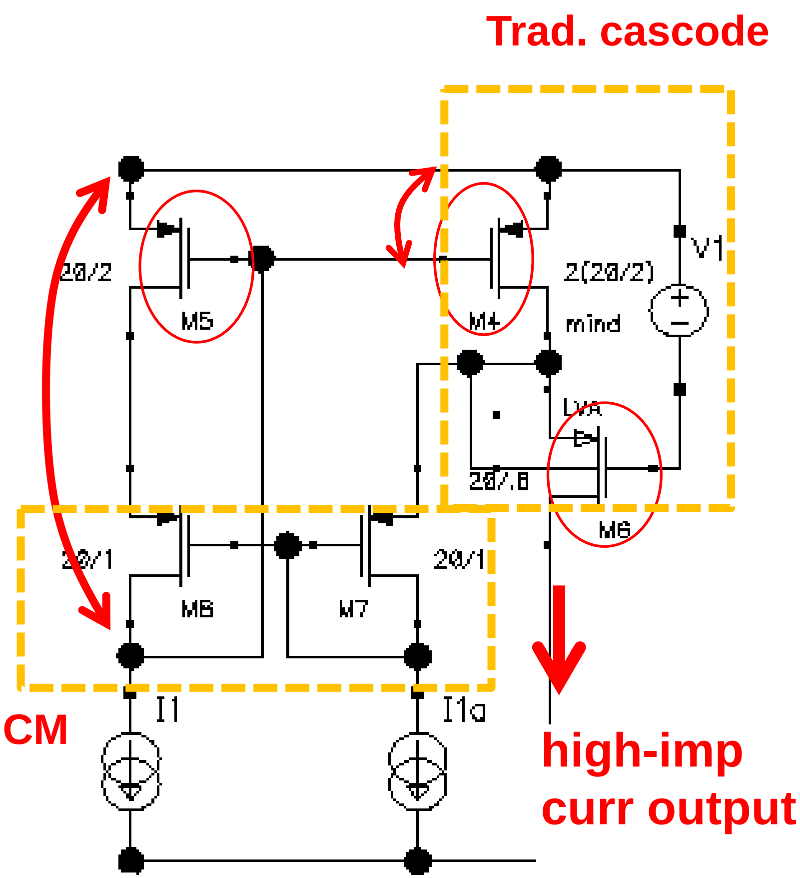
the CM enhances the impedance seen by Src of M1

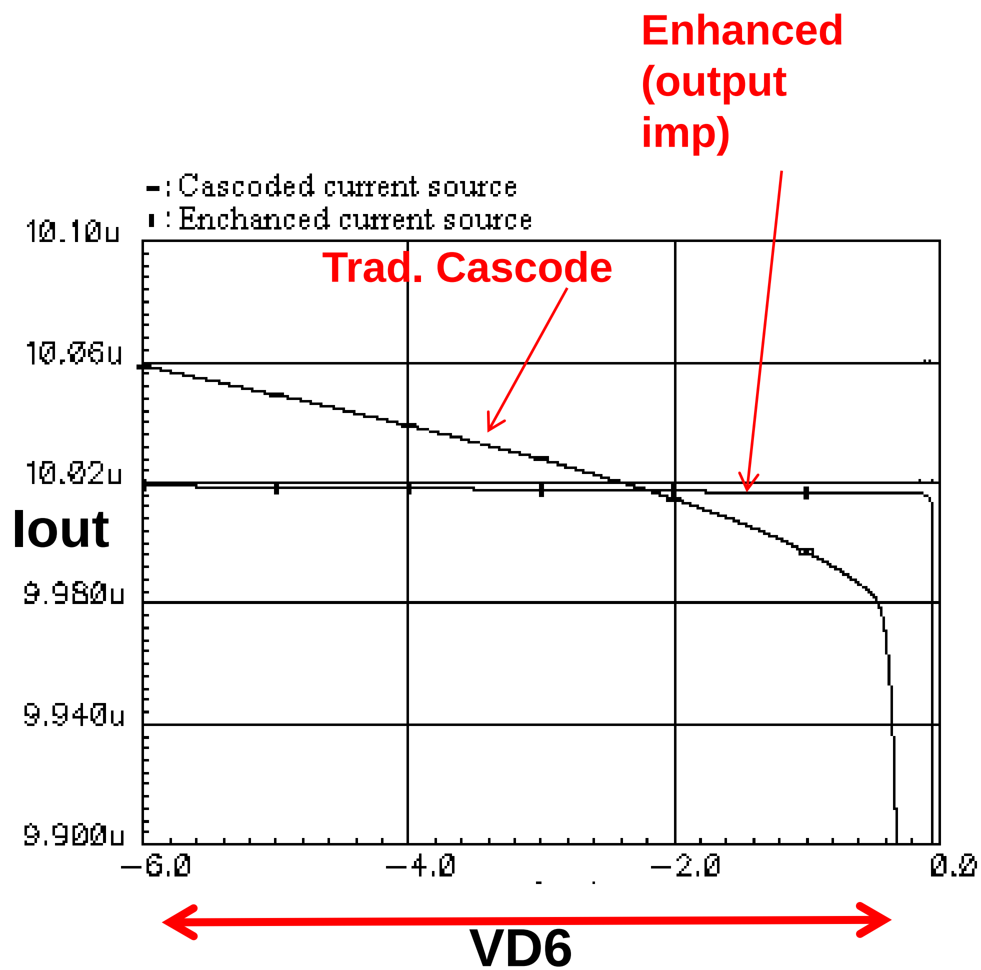
High Output Impedance

- **This configuration is very useful;**
- **A current mirror/amplifier with very high output impedance.**
- **M1 is common gate; the output impedance depends on** *the impedance at the* ***source of M1*****.**
- **For a <u>simple cascode</u> the source impedance would be equal to rd0 of M0 ➔ output impedance = rd0(gm1xrd1).**
- **But due to addition of the <u>current amplifier (M7-M8)</u>, the impedance seen by the source of M1 becomes rd0x(gm8xrd8) x(gm1xrd1), a much higher impedance.**

Example 2 (cont'd, P-channel Implem.)

PMOS configuration



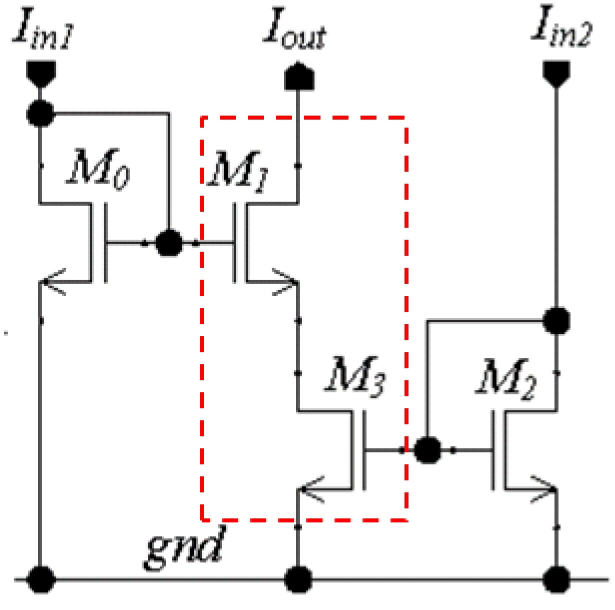


Wider range of hi imp

(Comments)

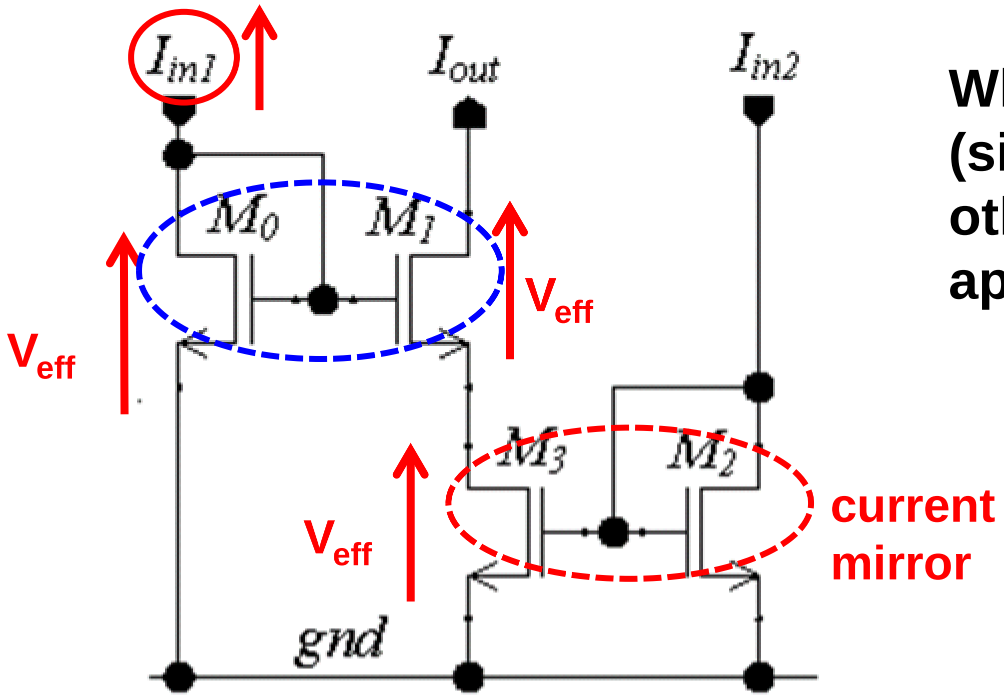
- **The high output impedance exists for a wider range of the voltages at the drain of M6;**
- **even when transistors M4 and M5 are entering the triode range of operation, the gain of the current amplifier M6, M7 is still high.**
- **The circuit is functioning even if transistor M6 enters into triode operation;**
- **The circuit stops functioning when the voltage at the drain of M6 is within 100 mV from the power supply voltage.**

Example 3: Max / Min Current Selector



Iout = min(Iin1, Iin2), if Iin1 ≠ Iin2 with large difference

Minimum current selector



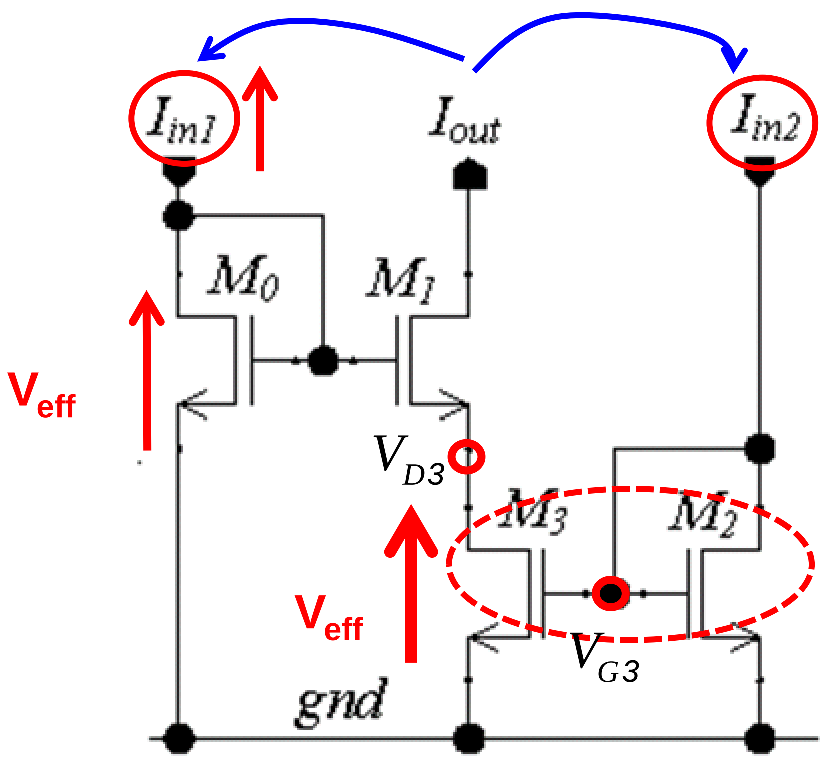
When both currents are equal, i.e., $I_{in1} = I_{in2}$, the output current $I_{out} = I_{in1} = I_{in2}$ (verify it!).

When one of them increases (significantly larger than the other), the output current approximates the smaller one.

(See next page)

K.-J. de Langen, and J.H. Huijsing, Compact Low-voltage and High-speed CMOS, BiCMOS and Bipolar Operational Amplifiers, Kluwer, 1999

Min Current Selector – How does it work?

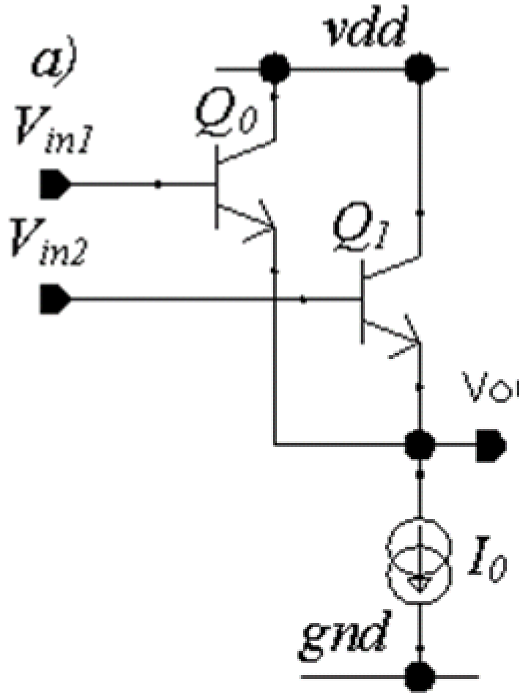


CM: Current Mirror

If I_{in1} >> I_{in2}, the voltage drop across M0 goes high, increasing the gate voltage of M1 ➔ M3 moves out of triode operation (VD3 rises) ➔ the CM M3-M2 functions, providing $I_{out} = I_{in2}$.

If I_{in2} >> I_{in1}, ➔ M3 enters triode operation (∵VG3 goes high) and M3 is ON (ro3 small) ➔ Then M0-M1 function as CM and $I_{out} \approx I_{in1}$ (the smaller).

Bipolar Min/max Selector



Bipolar min/max voltage selector :
Vo = min(Vin1, Vin2)

(bipolar transistors can be replaced by MOSFETs)

Please simulate this circuit.

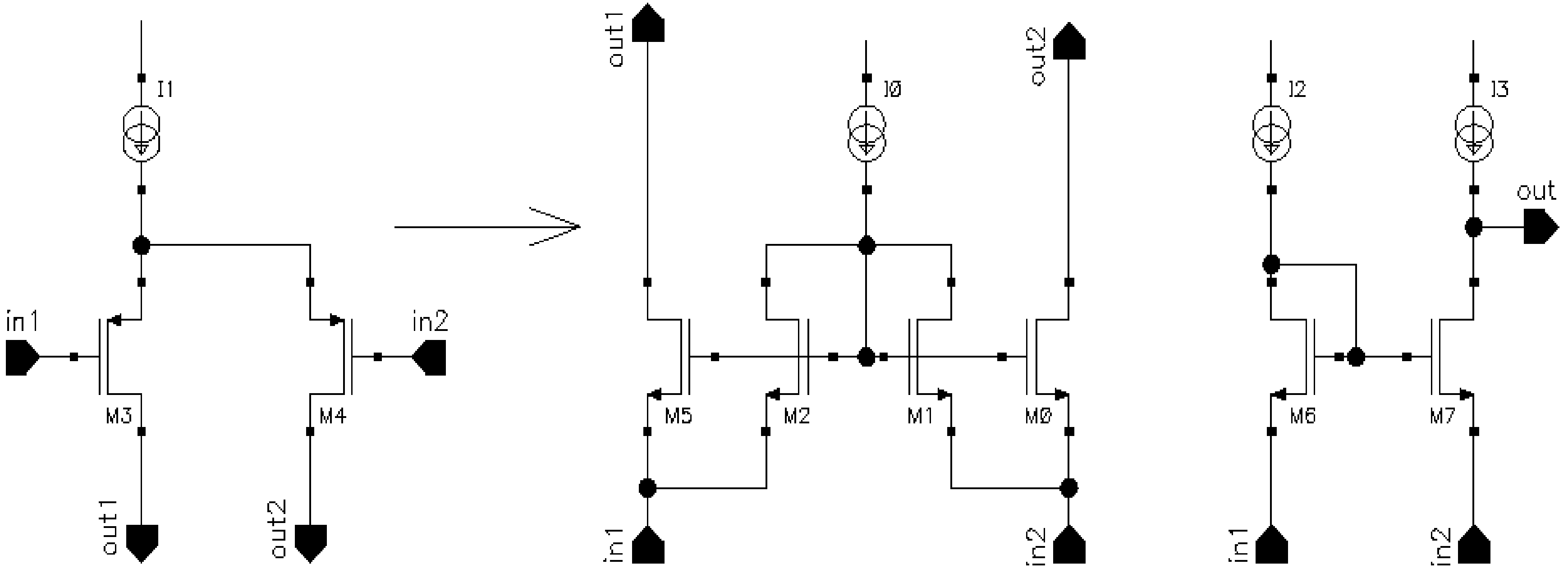
Reference

- **This lecture has made reference to Prof. Igor Filanovsky's tutorial lecture on opamp design.**
- **He presented it during a tutorial session on the Midwest Symp. CAS in Seoul, 2011.**

Appendix

p-Channel Cells

The counterpart cells using p-channel (PMOS) transistors



Current mirror

Symmetric current amplifier

Asymmetric current amplifier