Lecture 8
gm/ID Sizing Method

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Preface

- **This lecture was based on the following paper:**
  - **F. Silveira, D. Flandre, and P. G. A. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE J. Solid-State Circuits, vol. 31, pp. 1314–1319, Sep. 1996*.**

Outline

- Intrinsic gain stage
- gm/ID in different regions
- gm/ID versus normalized current (ID/(W/L))
- gm/ID sizing procedure
- Experimental result
- SOI technology for low-power circuits
- Summary

Tradeoff btw Power & Speed

- **CMOS analog circuits traditionally work in strong inversion (saturation)**
- **Weak inversion region → minimum power consumption; but slow**
- **Moderate inversion → good compromise in power and speed (future design interest)**
- **Design challenges:**
  - **Requiring both low power and high speed**

Traditional Design Methodology

- Traditional optimization approaches → SPICE plus numerical optimization software
  - Disadvantage: lack of design insights
- Main stream methods emphasize "strong inversion";
- Micropower design techniques exploit known "weak inversion" models.
- Symbolic or simple hand-calculation methods → better insights,
  - But lack simple and accurate hand models for moderate inversion

The gm/ID Methodology

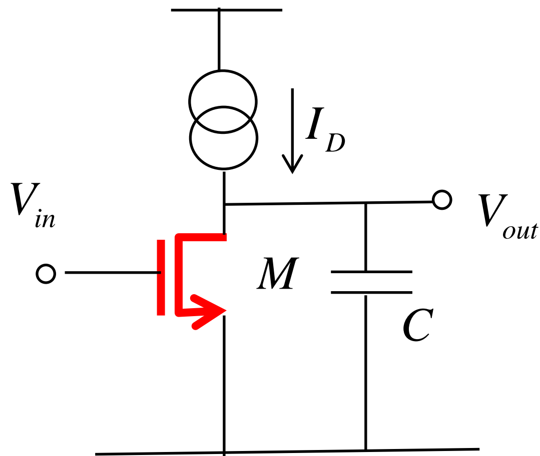
- **One single model that works in all operation regions.**
- **Focused on g_m/I_D ratio versus the normalized current $I_D/(W/L)$**
  - **the normalized current $I_D/$ (W/L) is characterized experimentally**
  - **or fitted with simple analytical models**

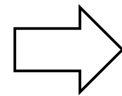
- **Helps design in moderate inversion for *low-power circuits***
  - **Offering good compromise between speed and power.;**
  - **power lower but speed not bad!**

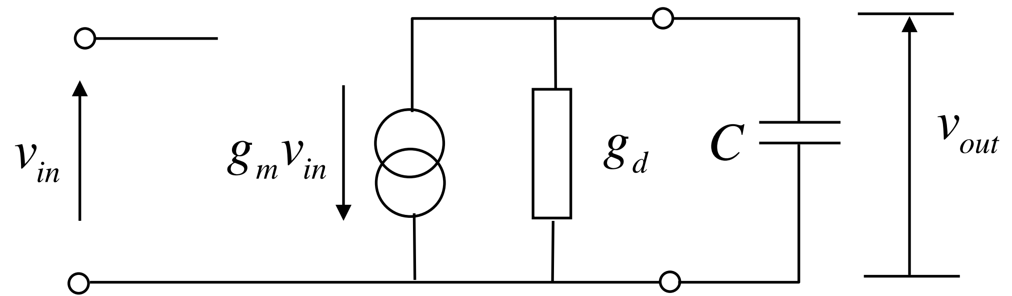
Motivation of gm/ID

- **gm/ID is a measure of the efficiency to translate current (i.e., power) into gm (i.e., gain).**
  - **The greater gm/ID, the greater gm is for a fixed ID.**
  - **gm/ID is interpreted as a measure of the "gm enhancement efficiency".**
- **It is strongly related to the performance of analog circuits.**
- **It also gives an indication of the device operating region.**
- **It can be used for transistor sizing.**

Intrinsic Gain Stage (I.G.S.)





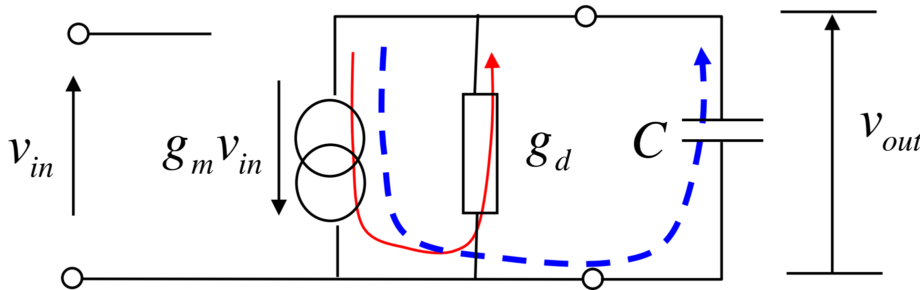


The common source transistor M is in saturation

The equivalent small-signal circuit

GBW

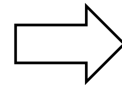
Gain-Bandwidth Product (GBW)



$$V_{out}(s) = H(s) V_{in}(s)$$

DC gain:

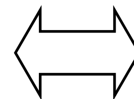
$$g_m v_{in} = -g_d v_{out}$$



$$H_{DC} = H(0) = \frac{v_{out}}{v_{in}} = -\frac{g_m}{g_d}$$

High freq gain:

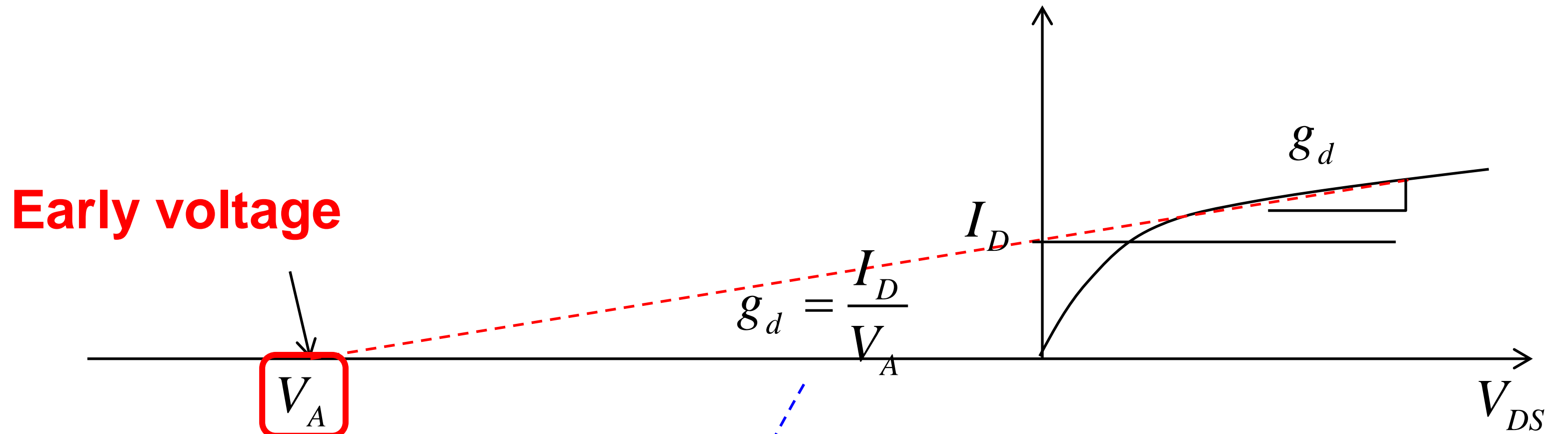
$$g_m v_{in} = -j\omega C v_{out}$$



$$H(j\omega) = \frac{v_{out}}{v_{in}} = -\frac{g_m}{j\omega C}$$

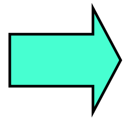
- At high frequencies, most of the current flows by the capacitor C.

Channel Length Modulation



$$\frac{v_{out}}{v_{in}} = -\frac{g_m}{g_d}$$

The Early voltage V_A controls the transistor small-signal output conductance, $g_d = I_D/V_A$.



$$A_{DC} = H(0) = \frac{v_{out}}{v_{in}} = -\frac{g_m}{g_d} = -\frac{g_m}{I_D} V_A$$

GBW (cont'd)

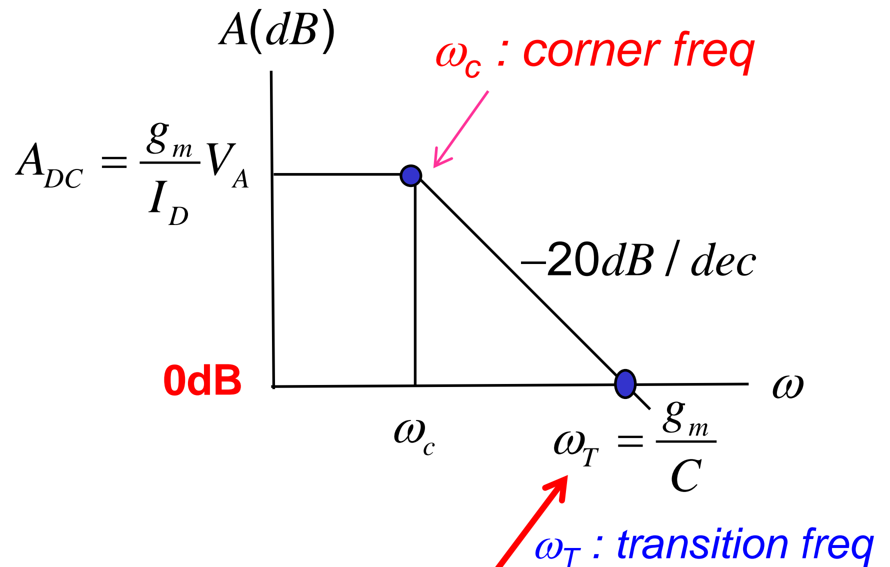
$$\begin{cases} H(0) = -\dfrac{g_m V_A}{I_D} \\ H(j\omega) = \dfrac{v_{out}}{v_{in}} = -\dfrac{g_m}{j\omega C} \end{cases}$$

at corner freq

$$A_{DC} = \left|H(s)\right|_{s=0} = \left|H(s)\right|_{s=j\omega_c}$$

$$\Rightarrow \frac{g_m V_A}{I_D} = \frac{g_m}{\omega_c C}$$

$$\Rightarrow \frac{V_A}{I_D} = \frac{1}{\omega_c C} \qquad \omega_c = \frac{I_D}{C V_A}$$



$$\omega_T = \omega_c A_{DC} = \frac{g_m}{C}$$

GBW

Calculation of gm/ID

The expression for gm/ID is derived as follows:

$$\frac{g_m}{I_D} = \frac{1}{I_D}\underbrace{\frac{\partial I_D}{\partial V_G}} = \frac{\partial \ln I_D}{\partial V_G} = \frac{\partial \ln\left\{\frac{I_D}{\left(\frac{W}{L}\right)}\right\}}{\partial V_G}$$

Called normalized drain current

$$I_{\square} \equiv \frac{I_D}{\left(\frac{W}{L}\right)}$$

ID normalized by the transistor size.

The derivative is maximum in the weak inversion (WI) region where the dependence of I_D versus V_G is exponential.

$$I_D = I_0 \exp\left(\frac{V_G}{nU_T}\right)$$

$$\ln\left(\frac{I_D}{I_0}\right) = \frac{V_G}{nU_T}$$

Quadratic MOS Models

The connections between ID, the W/L ratio, and gm can be derived from the transistor large-signal model.

The classical MOS model is defined for the three regions:

1) Strong inversion region (Quadratic Model):

- **When $V_{ov} = (V_G - V_{th}) > 0.2V$.**

2) Moderate inversion region;

3) Weak inversion region: Once the current approaches $I_{D,min}$ (see the lecture on EKV), W/L must be increased fastly to further increase the DC gain.

Quadratic model in Strong Inversion

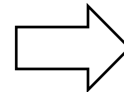
The quadratic expression of ID for a MOS transistor in saturation:

$$I_D = \beta \frac{(V_G - V_{th})^2}{2n}$$

n is the slope factor ≈ 1

$$\beta = \mu C_{ox} \frac{W}{L}$$

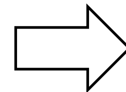
$$g_m = \frac{\partial I_D}{\partial V_G} = \beta \frac{V_G - V_{th}}{n} = \sqrt{\frac{2\beta I_D}{n}}$$



$$\frac{W}{L} = \frac{n g_m^2}{2\mu C_{ox}} \cdot \frac{1}{I_D}$$

We also have

$$g_m = \sqrt{\frac{2\beta I_D}{n}} = \frac{\beta}{n}(V_G - V_{th})$$



$$\frac{g_m}{I_D} = \frac{2}{(V_G - V_{th})}$$

Indep. of (W/L)

ID is proportional to β (hence W), so is gm.

(cont'd)

$$\frac{W}{L} = \frac{ng_m^2}{2\mu C_{ox}} \cdot \frac{1}{I_D}$$

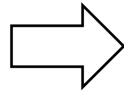
$$\frac{\frac{W}{L}}{I_D} = \frac{n}{2\mu C_{ox}} \cdot \frac{g_m^2}{I_D^2} = \frac{n}{2\mu C_{ox}} \cdot \left(\frac{g_m}{I_D}\right)^2$$

$$\frac{g_m}{I_D} = \sqrt{\frac{2\mu C_{ox}}{n}} \frac{1}{\sqrt{I_D / \frac{W}{L}}}$$

gm/ID is inversely proportional to the sqrt of the normalized ID.

Relation in strong inversion

$$\frac{W}{L} = \frac{n g_m^2}{2\mu C_{ox}} \cdot \frac{1}{I_D}$$



$$\log \frac{W}{L} = \left(\log \frac{n g_m^2}{2\mu C_{ox}} \right) - \log I_D$$

Approx const in strong inversion

sizing I.G.S. in weak, strong inv. (blue) and E.K.V model (red)

GVO (V)

-0.2

-0.1

0

0.1

0.2

0.3

0.4

DC gain

Strong inversion asymptote

Weak inversion asymptote

W / L

log(W/L)

I_D (A)

log(ID)

ID → small

$$A_{DC} = \frac{g_m V_A}{I_D}$$

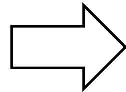
(derived for the Intrinsic Gain Stage)

- **It seems that the DC gain would increase to infinite as the drain current goes to 0.**
- **However, as the current diminishes, the transistor enters moderate and weak inversion, where the quadratic model for the drain current fails.**

Weak Inversion

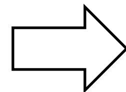
The drain current in weak inversion is given by the exponential I-V relation:

$$I_D = I_0 \exp\left(\frac{V_G}{nU_T}\right)$$



$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{I_D}{nU_T}$$

i.e., gm/ID is approx. const in weak inversion.



$$I_{D,\min} = nU_T g_m$$

where n is the subthreshold slope factor and U_T the thermal voltage.

In weak inversion, the drain current ID alone determines gm, which in turn determines the GBW.

$$GBW = 2\pi f_T = \frac{g_m}{C}$$

(for I.G.S.)

Moderate Inversion Region

The candidate model for moderate inversion is (see Jespers 2010, Chapter 4):

$$\frac{W}{L} = \frac{n g_m^2}{2\mu C_{ox}} \frac{1}{(I_D - I_{D,\min})}$$

The expression is valid in all regions, from strong to weak inversion.

***Exercise*: Design an I.G.S. with**

- **load C = 1 pF;**
- **transition frequency f_T = 100 MHz;**
- **μC_{ox} = 4x10^{-4} AV^2 ;**
- **slope factor n = 1.2;**
- **Early voltage V_A = 10V .**

Figure

Plot of aspect ratio W/L vs ID of an (ideal) Intrinsic Gain Stage.
The numbers besides the RED circles show the *Overdrive Gate Voltage*
$V_{ov} = (V_G - V_{th})$.

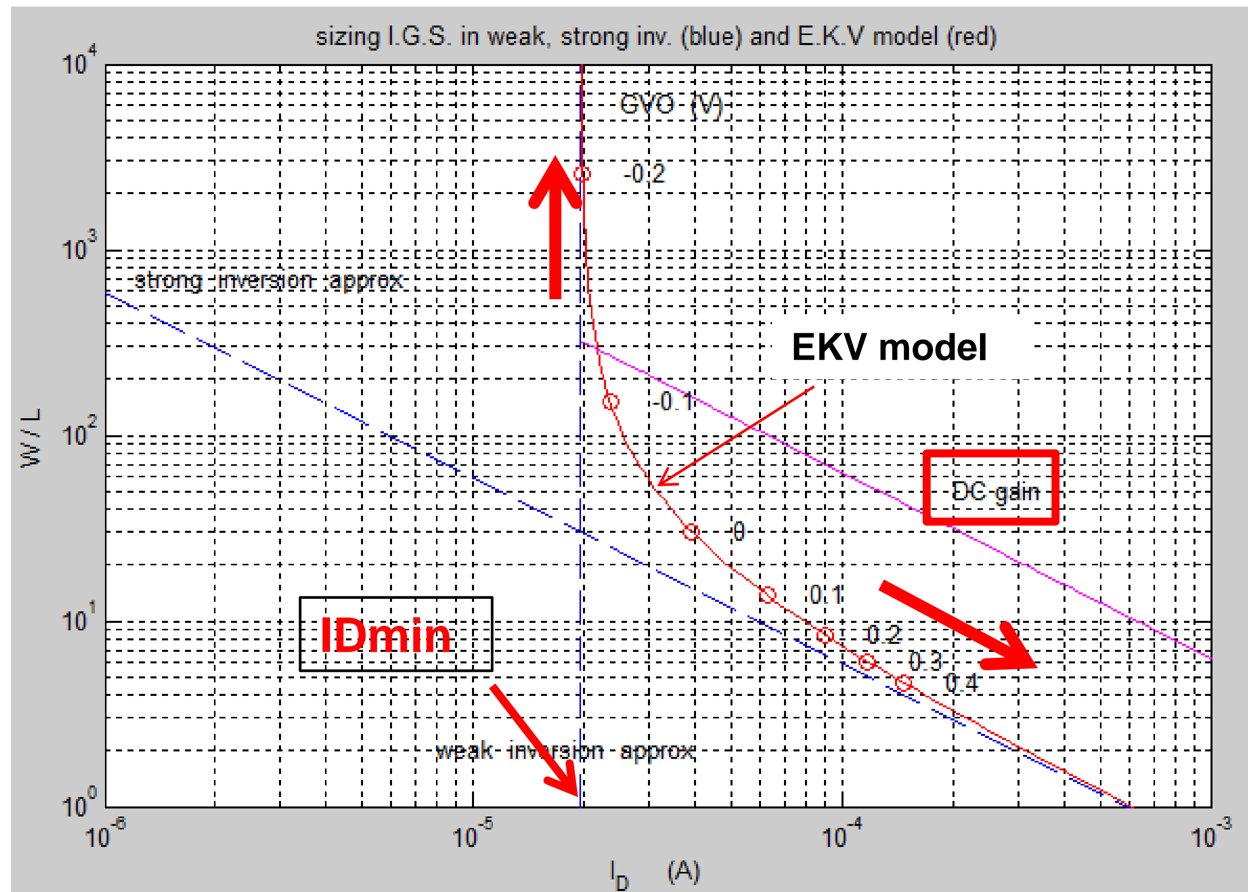
This figure displays (W/L) vs ID achieving the desired GBW (i.e., const f_T or gm).

$$A_{DC} = -\frac{g_m}{I_D} V_A$$

for ID large

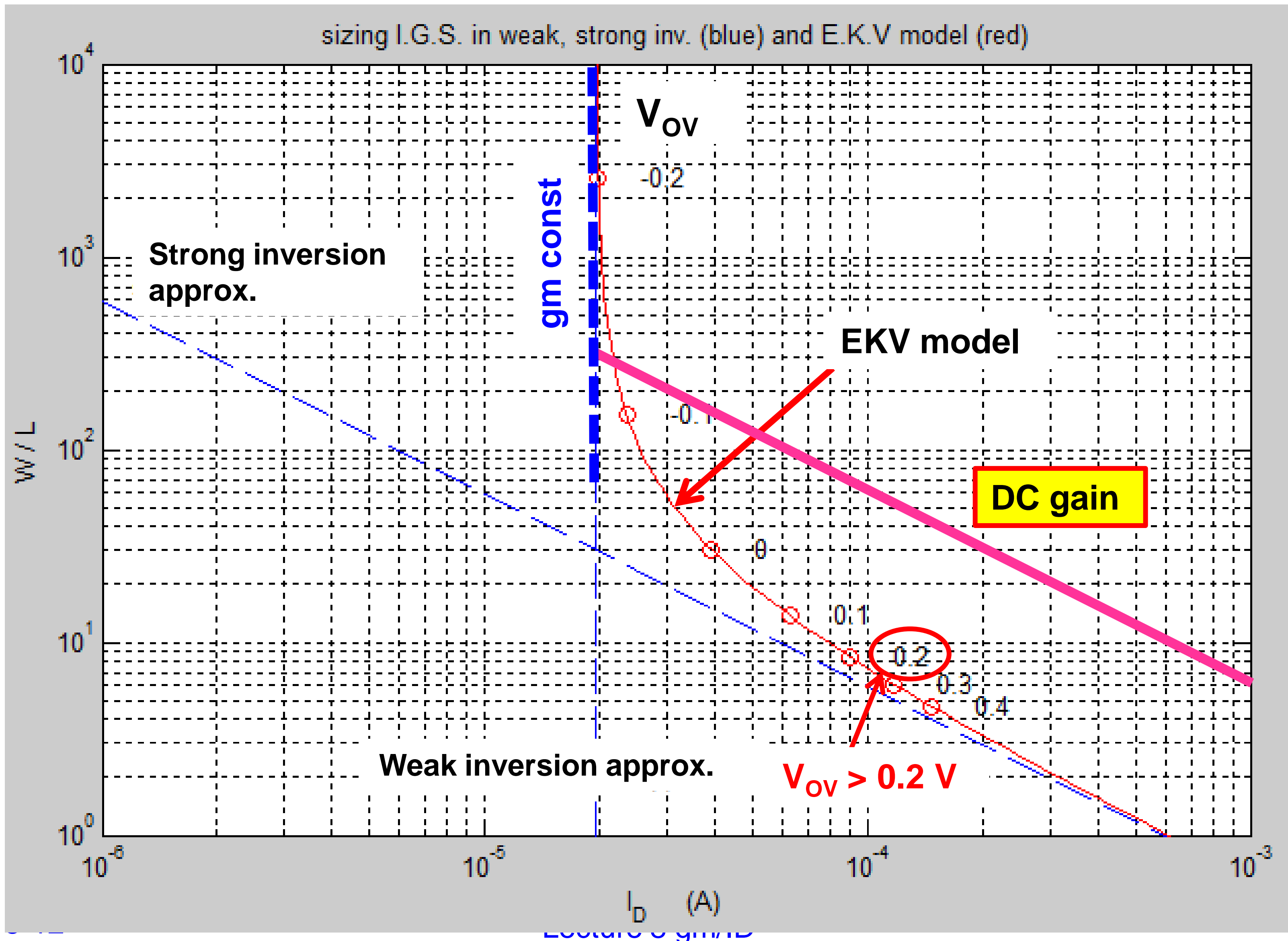
$$\log A_{DC} = \log(-g_m V_A) - \log I_D$$

(gm ~ const)



W/L versus ID

(See comments next page)



Comment on the Figure

We see that the DC gain varies like the reciprocal of I_D;
➔ Smaller drain current, larger DC gain.

The largest DC gain is arrived at when ID reaches the minimum $I_{D,min}$.

The DC gain is approximated by the equation considering Early voltage:

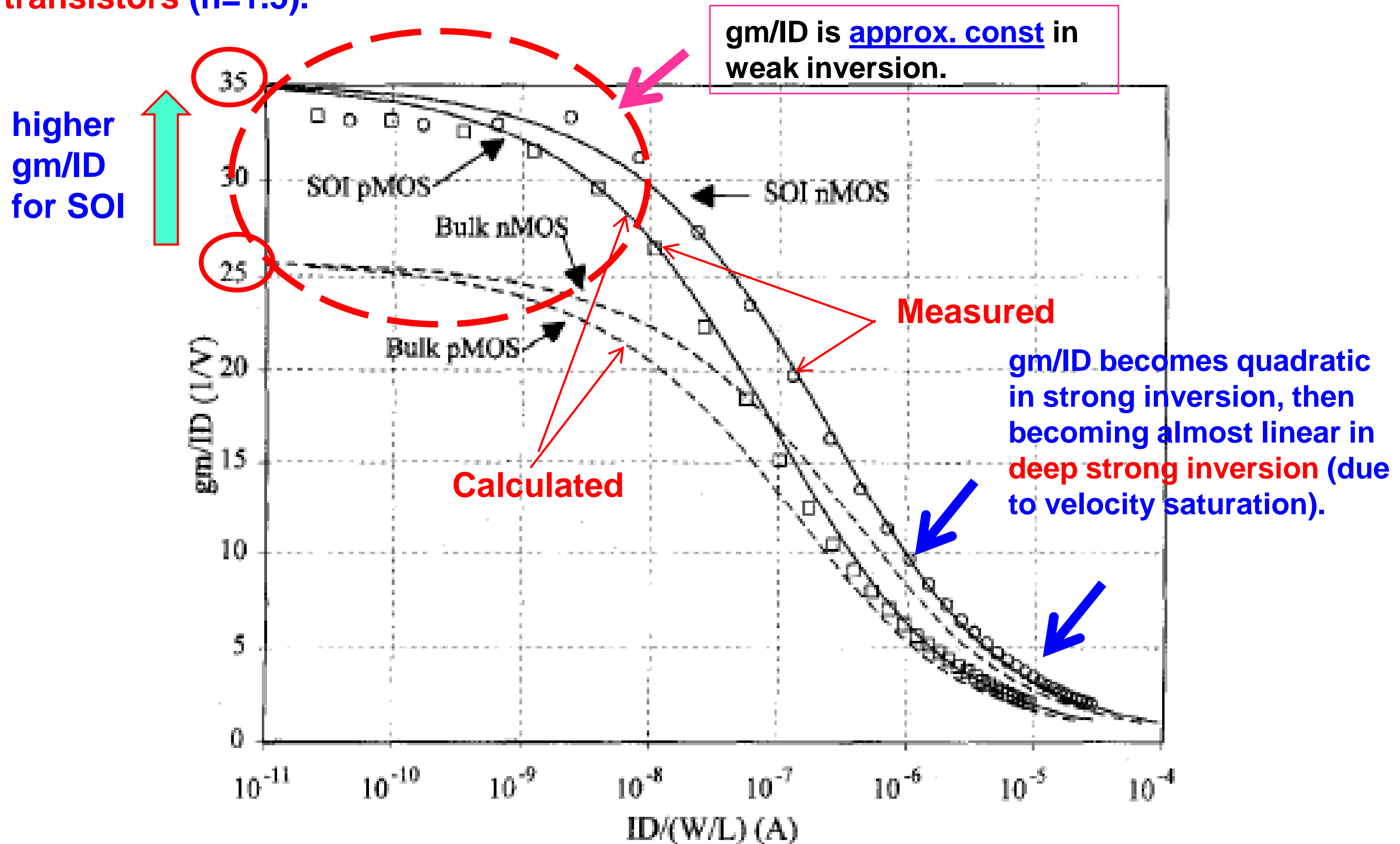
$$A_{DC} = -\frac{g_m}{I_D} V_A$$

When $I_D = I_{D,\min} = g_m n U_T$

➔ the max DC gain:

$$A_{DC,\max} = -\frac{V_A}{nU_T}$$

The thin-film SOI transistors (n=1.1) has increased subthreshold slope (due to smaller n), giving a maximum value of gm/ID of about 35 while only 25 for bulk transistors (n=1.5).



Calculated and measured gm/ID vs ID/(W/L) for bulk transistors and thin-film fully-depleted SOI transistors.

Observations

- gm/ID decreases when the normalized ID moves toward the strong inversion region.
- For the same gm/ID, $I_{\square,p}$ is lower than $I_{\square,n}$ due to the mobility difference.
  - Hence, requiring larger W/L for pMOS to achieve an equal ID.

- Hence, gm/ID is also an *indicator* of the transistor operation region.

- Both gm and ID are proportional to size;
- but gm/ID is size independent.
- Once any two values among gm/ID, gm, and ID are given, we can determine the aspect ratio W/L.

gm/ID vs normalized current

- The normalized current ($I_{\square}$ = ID/(W/L)) is independent of the transistor size.
- The relationship between gm/ID and $I_{\square}$ is a unique characteristic for one type of transistors.
  - However, this statement has to be revised when dealing with short channel transistors.

- The characteristic of (gm/ID) vs $I_{\square}$ can be explored extensively during the design phase
- The actual gm/ID vs $I_{\square}$ can be obtained by either analytical method (fitting) or measurement.

gm/ID Characterization

- **Two characterization methods: semi-empirical or model-driven.**
- **1) Semi-empirical: it makes use of real measurements or data derived from advanced MOS models.**
- **2) Model-based: it applies simple models with reliable analytical expression.**
  - **The basic EKV model is a candidate but not perfect;**
  - **The EKV parameters are allowed to vary with bias conditions and gate lengths.**

gm/ID Characterization

- **In order to take into account of process variations,**
- **it is more appropriate to consider averaged curves which are representative of a large number of transistors**

Accurate Reference Models

- **BSIM is a widely used state-of-the-art model available in the public domain.**
  - **It is based on threshold voltage formulations;**
  - **But has weaknesses (model inaccuracy) in moderate inversion.**

- **PSP model from Penn State University and Philips (now NXP) is considered the more accurate industrial standard.**
  - **Based on the surface potential model (like the Charge Sheet Model of EKV).**

gm/ID Sizing Procedure

gm/ID Sizing Procedure

We derived from the quadratic model:

$$\frac{g_m}{I_D} = \frac{2}{V_{GS} - V_{th}}$$

$g_m \sim I_D \sim W$

➔ (gm/ID) is independent of the gate width (W)

•Determine g_m according to (GBW = f_T): $g_m = 2\pi f_T C$

•Determine I_D by the const gm/ID equation: $I_D = g_m \Big/ \left(\frac{g_m}{I_D}\right)^*$

The reference ratio (gm/ID)* is obtained from a similar device whose W* and L* are known.

•Determine the device size (W) by the proportionality btw ID and W:

$$W = (W)^* \frac{I_D}{\left(I_D\right)^*}$$

The reference (gm/ID)*

The **reference (gm/ID)*** is defined by:

$$\left(\frac{g_m}{I_D}\right)^* = \frac{1}{I_D^*}\frac{dI_D^*}{dV_G} = \frac{d}{dV_G}\log(I_D^*)$$

Two typical methods:

1. **Semi-empirical gm/ID sizing method: Deriving the reference (gm/ID)* from experimental $I_D(V_{GS})$ characteristics (typically from advanced models such as BSIM or PSP).**

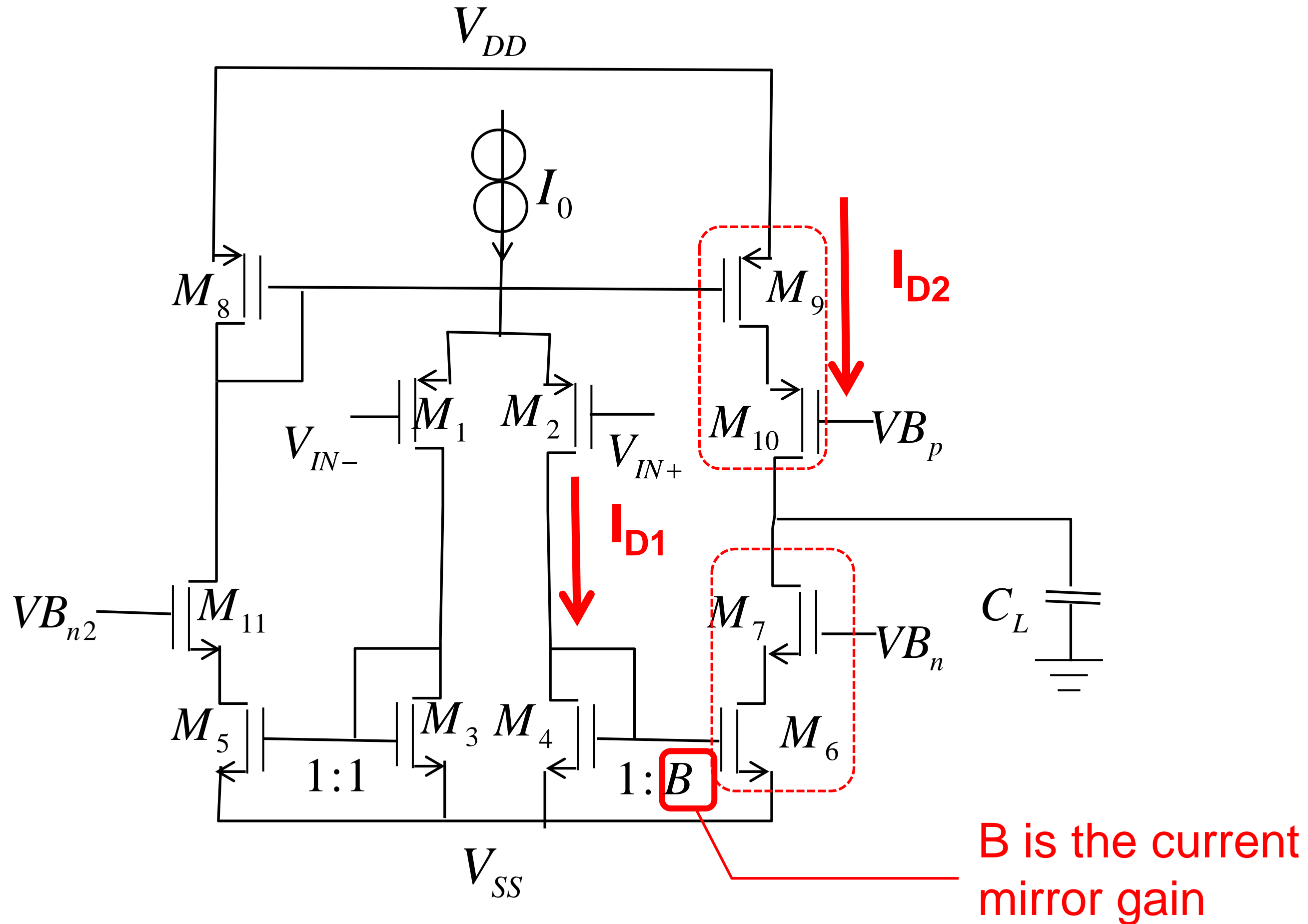
2. **Model-based method: Deriving (gm/ID)* from analytical large signal model adequately accurate by parameter fitting (e.g., EKV model).**

Application to OTA Synthesis

Cascode OTA, CMOS-SOI technology

Application

Synthesize a cascode OTA by the gm/ID method:



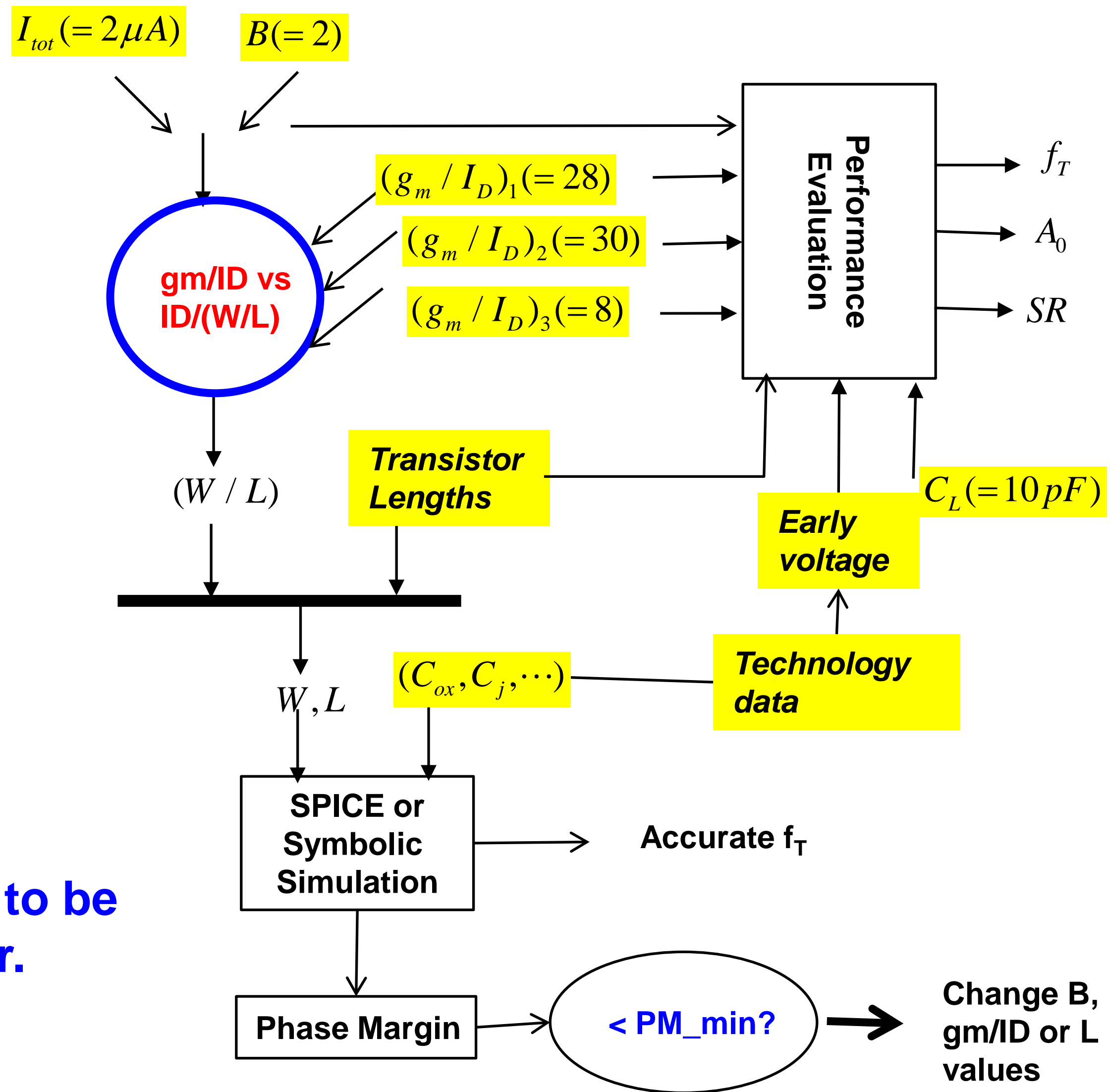
OTA schematic (to be implemented CMOS-SOI)

OTA Synthesis

- Assume total supply current is $I_{tot} = 2\ \mu A$, load capacitor is $C_L = 10pF$, and supply voltage $V_{DD} = 3$ V.
- Design to achieve the best performance of:
  - Open loop dc gain (A_{DC}),
  - Transition frequency (f_T),
  - Phase margin (PM), and
  - Slew rate (SR)

- It is straightforward to take into account of other performance aspects (like noise or common mode rejection) as long as they are directly related to the current and small-signal parameters.
- For large-signal performance such as signal swing, an "I_D vs V_G" or "gm/I_D vs V_G" relationship is required.

gm/ID Design Flow



Highlighted are the data to be provided by the designer.

OTA Synthesis

The DC gain can be derived as:

$$A_{DC} = \left(\frac{g_m}{I_D}\right)_1 \left(\frac{g_m}{I_D}\right)_2 \frac{1}{\frac{1}{V_{A6} \cdot V_{A7}} + \frac{1}{V_{A9} \cdot V_{A10}}}$$

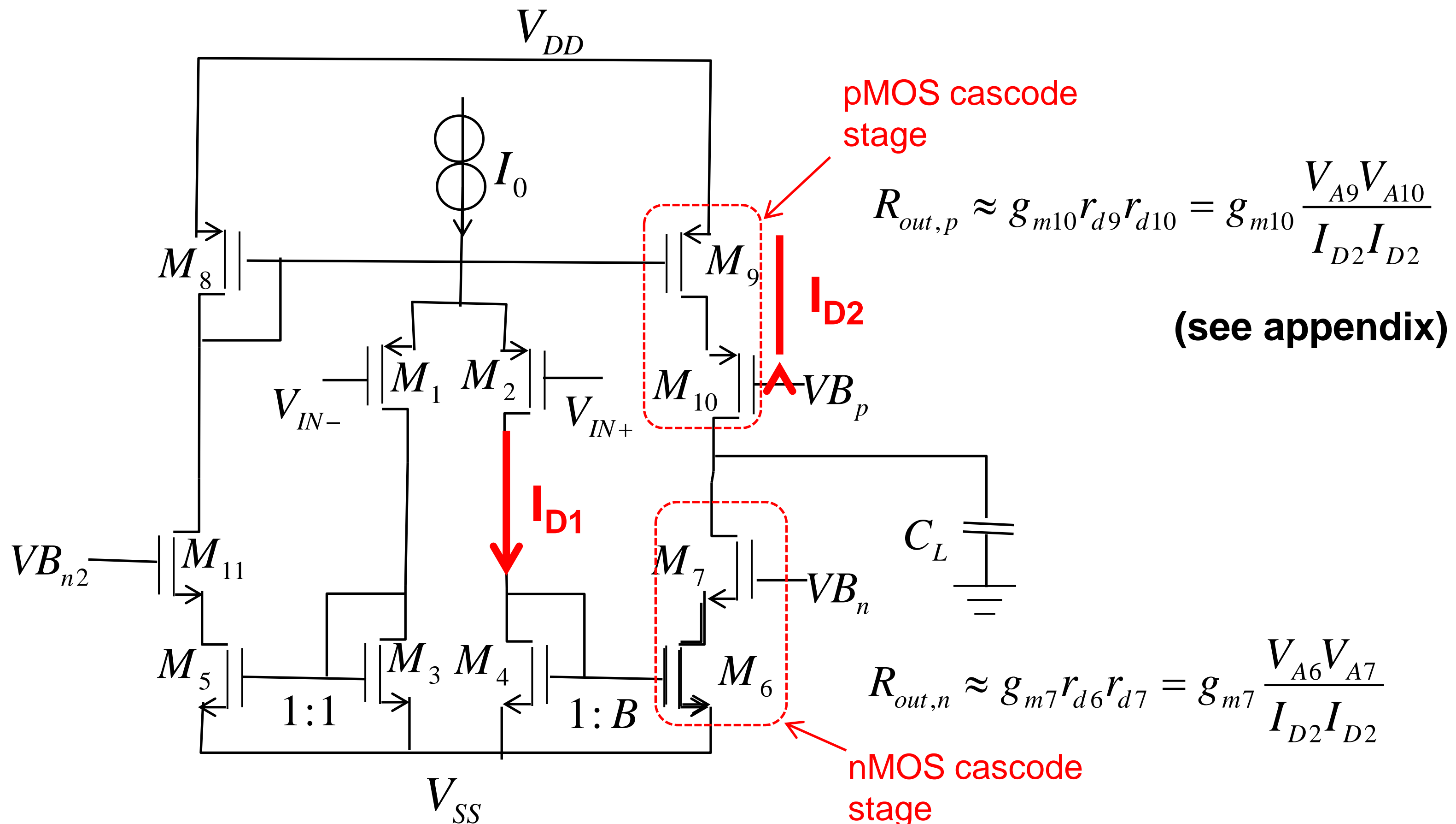
(to be derived next)

where $(gm/ID)_1$ is the ratio of the input transistors and $(gm/ID)_2$ is the ratio of the *cascode* transistors.
$V_{A6,7,9,10}$ are Early voltages.

The Early voltages are considered proportional to the transistor length with a typical constant proportionality of 7V/um. (In the paper L is in the rage of 3 to 12 um.)

Derivation of DC Gain

$$A_{DC} = \left(\frac{g_m}{I_D}\right)_1 \left(\frac{g_m}{I_D}\right)_2 \frac{1}{\dfrac{1}{V_{A6} \cdot V_{A7}} + \dfrac{1}{V_{A9} \cdot V_{A10}}}$$



$$R_{out,p} \approx g_{m10} r_{d9} r_{d10} = g_{m10} \frac{V_{A9} V_{A10}}{I_{D2} I_{D2}}$$

(see appendix)

$$R_{out,n} \approx g_{m7} r_{d6} r_{d7} = g_{m7} \frac{V_{A6} V_{A7}}{I_{D2} I_{D2}}$$

Derivation (cont'd)

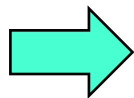
$$R_{out,p} \approx g_{m10} r_{d9} r_{d10} = g_{m10} \frac{V_{A9} V_{A10}}{I_{D2} I_{D2}}; \qquad R_{out,n} \approx g_{m7} r_{d6} r_{d7} = g_{m7} \frac{V_{A6} V_{A7}}{I_{D2} I_{D2}}$$

$$R_{out} = R_{out,p} \parallel R_{out,n} \approx g_{m10} \frac{V_{A9} V_{A10}}{I_{D2} I_{D2}} \parallel g_{m7} \frac{V_{A6} V_{A7}}{I_{D2} I_{D2}}$$

$$= \frac{g_{m7.10}}{I_{D2} I_{D2}} \frac{1}{\frac{1}{V_{A9} V_{A10}} + \frac{1}{V_{A6} V_{A7}}}$$

$$g_{m7,10} = g_{m7} = g_{m10}$$

gain of 1st stage



$$A_{DC} = g_{m1} R_{out} = \frac{g_{m1} g_{m7,10}}{I_{D2} I_{D2}} \frac{1}{\frac{1}{V_{A9} V_{A10}} + \frac{1}{V_{A6} V_{A7}}}$$

$$= \left(\frac{g_m}{I_D}\right)_1 \left(\frac{g_m}{I_D}\right)_2 \frac{1}{\frac{1}{V_{A9} V_{A10}} + \frac{1}{V_{A6} V_{A7}}}$$

Assuming current mirror ratio from the input stage to the cascode stage is 1:1.

(cont'd)

$$SR = \frac{B \bullet I_{D1}}{C_L}$$

$$f_T = \frac{B \cdot g_{m1}}{2\pi \cdot C_L}$$

1st order approximation of f_T

where B is the current mirror ratio, I_{D1} is the current of the first stage, and g_{m1} is the transconductance of the input transistor.

Set B = 2 in the paper.

The max B value is limited by its influence on the OTA stability.

f_T is also proportional to gm/ID, given fixed ID.

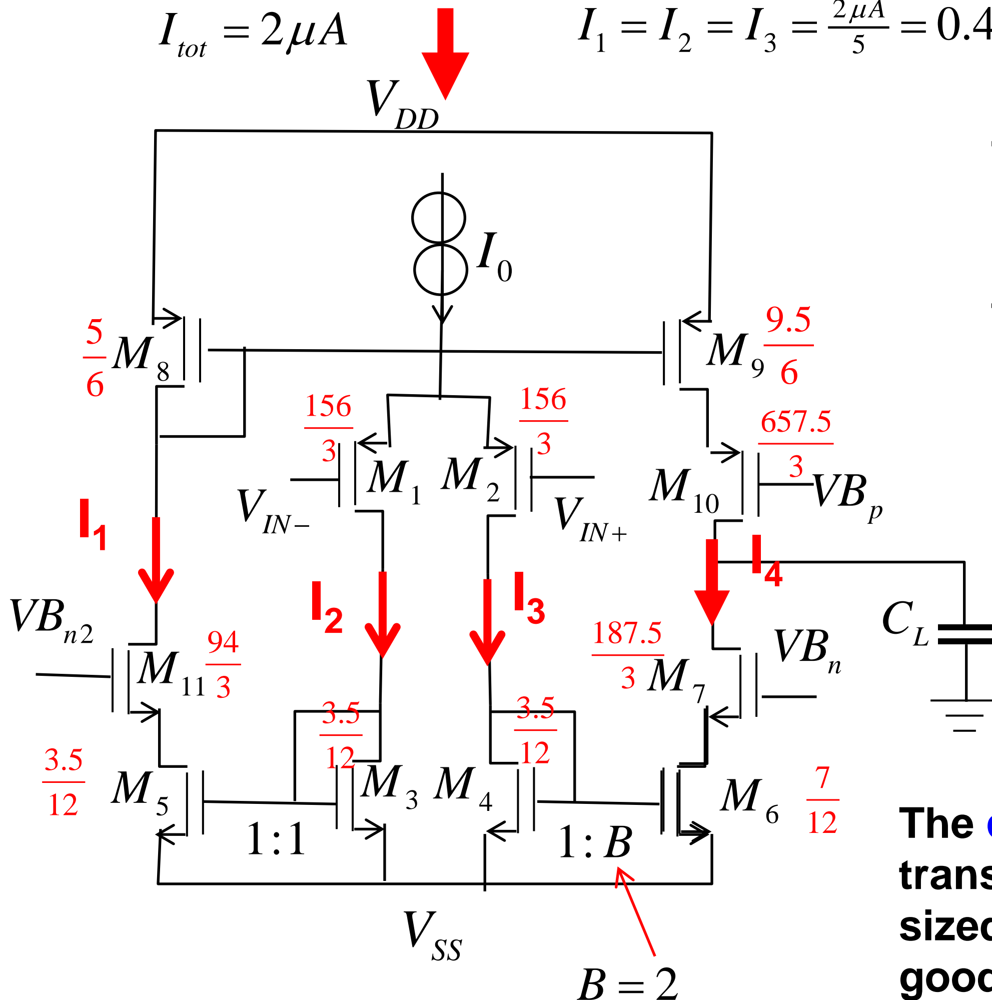
Sizing Procedure for the OTA

1. **Determine the drain current of each transistor according to the total supply current and the current mirror ratio B (= 2).**
2. **Choose gm/ID accordingly to their effect on the OTA performance,**
3. **Determine the normalized current according to the experimental curve of (gm/ID) vs $I_{\square}$.**
4. **Calculate W/L for each transistor.**

Sizing the OTA

The total current is divided into four branch currents (one branch doubled):

$$I_{tot} = 2\mu A \qquad I_1 = I_2 = I_3 = \tfrac{2\mu A}{5} = 0.4\mu A; \qquad I_4 = B \cdot I_3 = \tfrac{4\mu A}{5} = 0.8\mu A$$



The gm/ID values are determined after design space exploration (optimizing tradeoff btw dc gain and f_T for a given PM).

$$\left(\frac{g_m}{I_D}\right)_{1,2} = 28; \qquad \left(\frac{g_m}{I_D}\right)_{7,10} = 30;$$

(correspond to operation in the moderate inversion region close to W.I.)

The current mirror transistors (M3,4,5) are sized in S.I. to guarantee good matching and noise properties.

$$\left(\frac{g_m}{I_D}\right)_{3} = 8;$$

Choice of gm/ID

- The dc gain is proportional to gm/ID ➔ gm/ID higher better.
- f_T is proportional to gm, hence gm/ID (if ID is fixed). ➔ also gm/ID higher better.

- However,
- The max gm/ID is limited by the weak inversion value
  - about 35 V^{-1} for thin-film fully-depleted SOI MOS (higher);
  - about 25 V^{-1} for bulk CMOS
- Also limited by the stability requirement
  - because increasing gm increases the transistor sizes (W), (hence, the parasitic caps), reducing the phase margin.

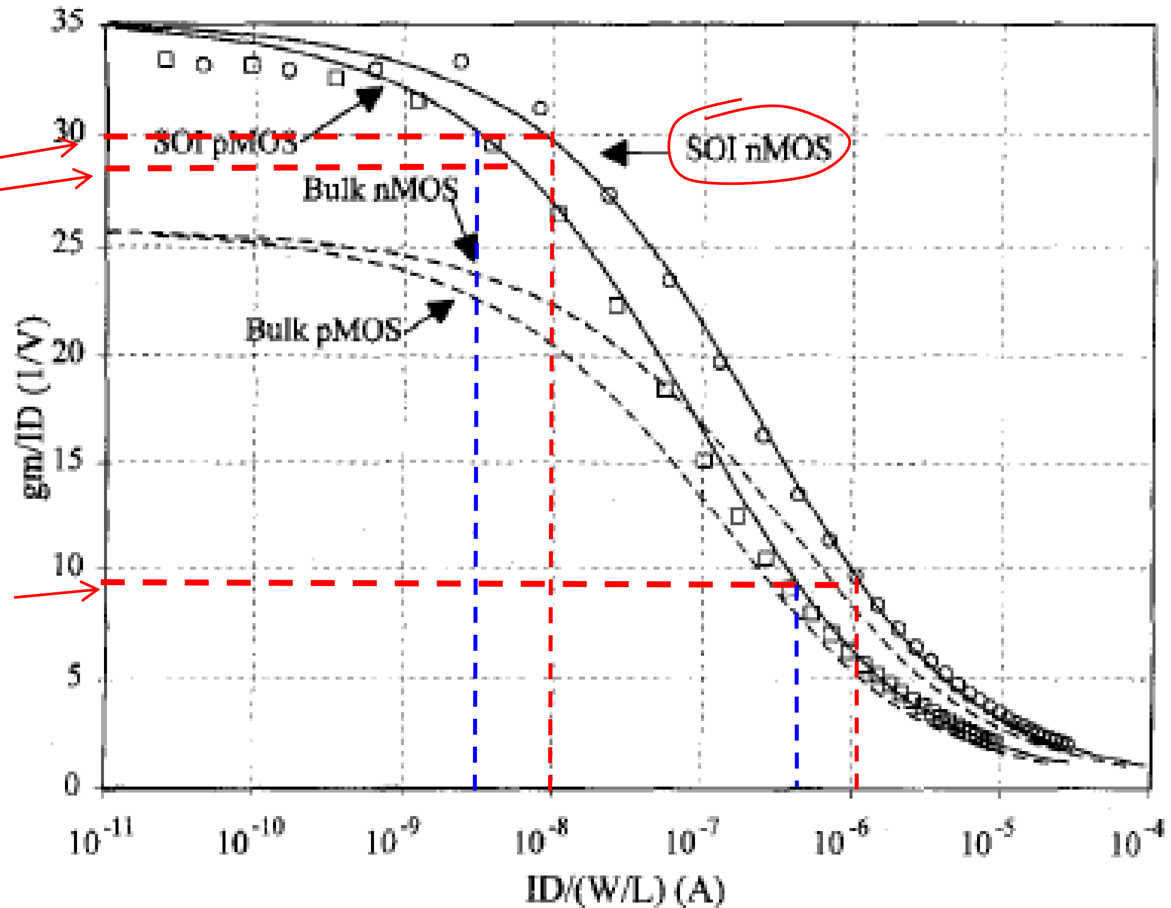
Looking up $I_{\square}$ from Curve

30

28

8

$\frac{g_m}{I_D}$



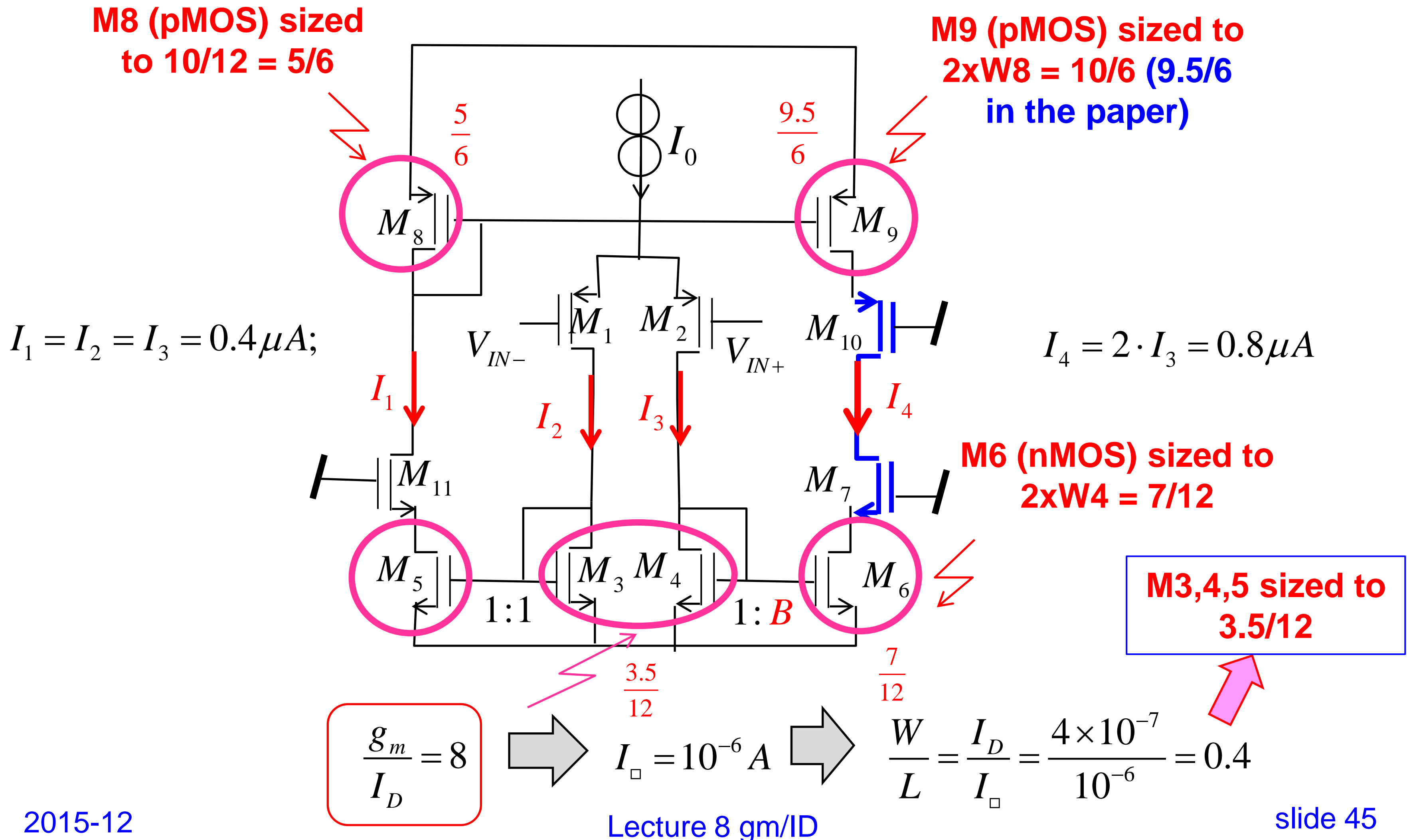
For nMOS, $I_{\square} \approx 10^{-8}$ for gm/ID = 30. For pMOS, $I_{\square}$ is smaller.

For nMOS, $I_{\square} \approx 10^{-6}$ for gm/ID = 8. For pMOS, $I_{\square}$ is smaller.

about 100x

Sizing Details - 1

1) Sizing the mirror transistors ...

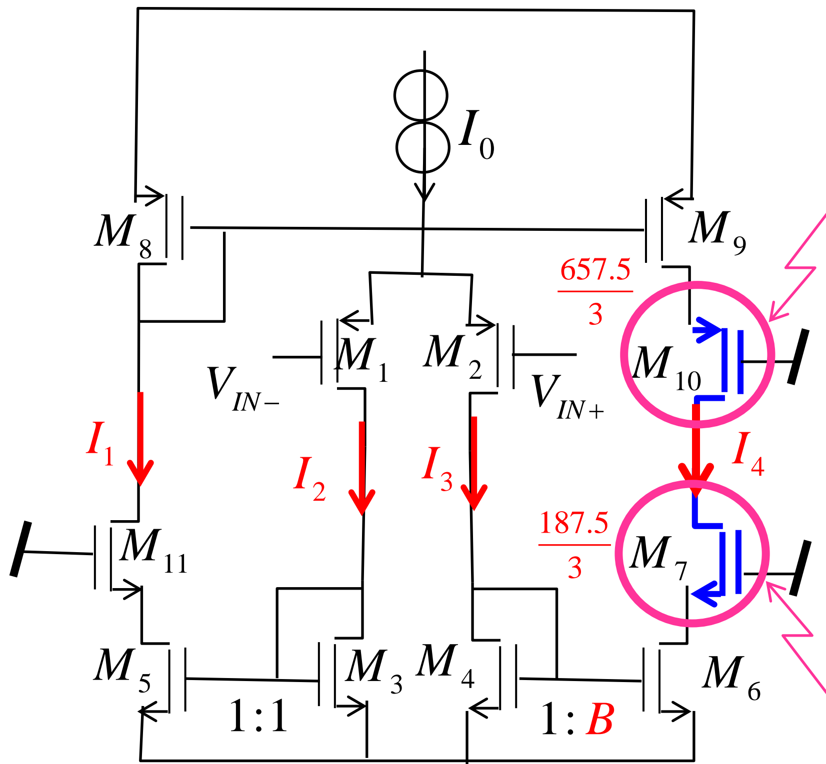


Sizing Details - 2

2) Sizing the cascode transistors (M7, M10) ...

$$I_1 = I_2 = I_3 = 0.4\mu A;$$

$$I_4 = 2 \cdot I_3 = 0.8\mu A$$



M10 (pMOS) sized larger to 657.5/3 = 219

$$\frac{g_m}{I_D} = 30$$

M7 sized to 187.5/3 = 62.5

$$I_{\square} = 10^{-8} A$$

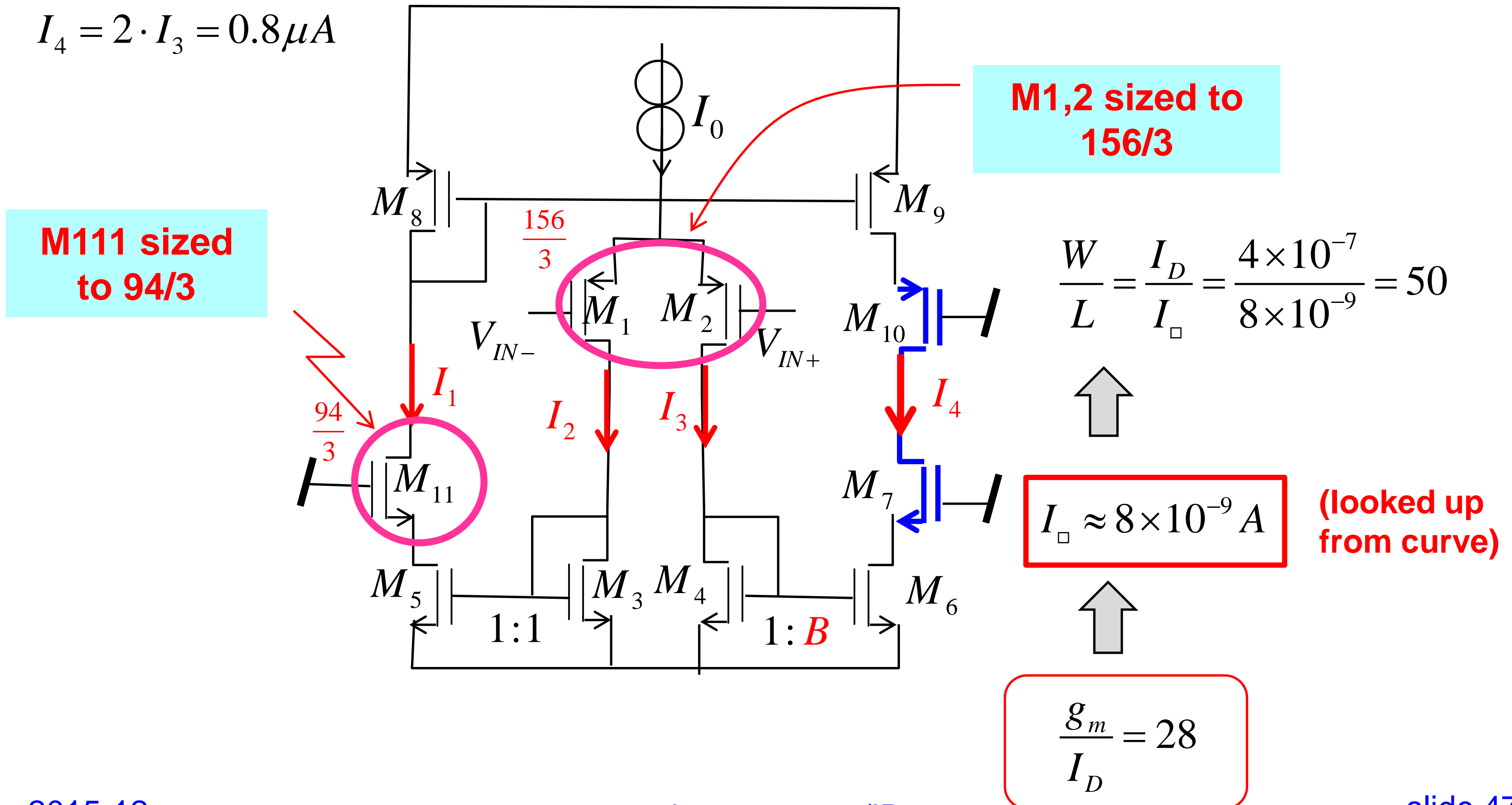
$$\frac{W}{L} = \frac{I_D}{I_{\square}} = \frac{8 \times 10^{-7}}{10^{-8}} = 80$$

Sizing Details - 3

3) Sizing the input transistors (M1,2) and M11 ...

$$I_1 = I_2 = I_3 = 0.4\mu A;$$

$$I_4 = 2 \cdot I_3 = 0.8\mu A$$



Summary of Transistor Sizes

The transistor lengths are determined by a trade-off btw area and stability, and dc gain (dependence of Early voltage on L). V_A ~ 7 (V/um) L empirically for L 3~12um.

TABLE I
OTA Transistor Dimensions

	W	L	Effective W/L
M1	156	3	57.6
M2	156	3	57.6
M3	3.5	12	0.26
M4	3.5	12	0.26
M5	3.5	12	0.26
M6	7	12	0.52
M7	187.5	3	69.3
M8	5	6	0.79
M9	9.5	6	1.58
M10	657.5	3	243.3
M11	94	3	34.6

Experimental Result

- **The sized OTA was realized in the 3-um CMOS-SOI process.**

TABLE Ⅱ. Calculated, simulated and measured results of OTA

	Synthesis Prog.	**HSPICE**	**Measurements**	Notes
$(gm/ID)_1$ (1/V)	28	29.4	28.3	
$(gm/ID)_2$ (1/V)	30	31.6	30.5	
A0 (dB)	**103.9**	105.5	103	
f_T (kHz)	324	336		@CL=10pF
PM (deg.)	72.5	72		@CL=10pF
f_T (kHz)	261*	270*	271*	@CL=12.3pF
PM (deg.)	63.8*	63*	60*	@CL=12.3pF
SR (V/us)	0.11	0.09	0.1	@CL=12.3pF
Output swing (Vpp)	2.02	2.2	1.93	@Vdd=3V

HSPICE uses level 34 model with a set of parameters optimized to fit the SOI MOSFET characteristics.

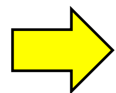
DC Gain Estimation

The open-loop dc gain can be estimated as follows:

$$A_{DC} = \left(\frac{g_m}{I_D}\right)_1 \left(\frac{g_m}{I_D}\right)_2 \frac{1}{\dfrac{1}{V_{A6}\cdot V_{A7}} + \dfrac{1}{V_{A9}\cdot V_{A10}}}$$

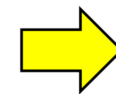
$$\left(\frac{g_m}{I_D}\right)_1 = 28V^{-1}; \qquad \left(\frac{g_m}{I_D}\right)_2 = 30V^{-1}; \qquad V_A \approx (7V/\mu m)\cdot L$$

L6 = 12; L7 = 3; L9 = 6; L10 = 3 um



$$A_{DC} = 49\times(28)(30)\frac{1}{\dfrac{1}{12\times 3} + \dfrac{1}{6\times 3}}$$

$$= 18\times 49\times(28)(30)\times\frac{2}{3} = 493{,}920$$



$$20\log_{10}(A_{DC}) = 113.8 \text{ dB}$$

~ HSPICE 105.5 dB

Comparison to Other Synthesis Methods

TABLE III. Comparison of results of gm/ID based synthesis with conventional **strong inversion (SI)** and **weak inversion (WI)** synthesis

	gm/ID method	SI synthesis.	SI real	WI synthesis.	WI real
$(gm/ID)_1$ (1/V)	28	28	18.7	35	30
$(gm/ID)_2$ (1/V)	30	30	19.7	35	30.5
A_0 (dB)	103.9	103.9	96.7	107.1	104.6
f_T (kHz)	324	351	236	395	344
PM (deg.)	72	84	86	64	68
W/L input pair	57.6	7.7	7.7	120.9	120.9
W/L cascode n	69.3	6.47	6.47	93.5	93.5
W/L cascode p	243.3	17.3	17.3	241.7	241.7
$\Sigma W \cdot L$ (um^2)	4900	1359	1359	6185	6185

Die area

By strong inversion (SI) synthesis, it overestimates fT by about 50% and the gain by about 7dB.
By weak inversion (WI) synthesis, it overestimates fT by 15% and the die area by 25%.

Comments on the comparison

- **The strong inversion (SI) synthesis extends quadratic expression to moderate inversion, this will *underestimate* transistor size (W/L), hence amplifier area.**

- **The weak inversion (WI) synthesis considers the exponential approximation for ID versus VG, it predicts the gm/ID equals to 35, independent of the current. The ID/(W/L) cannot be determined, it is chosen to guarantee weak inversion operation.**

- **Using the transistor sizes provided by the SI and WI synthesis, then referring to the real gm/ID versus ID/(W/L) data, the resulting estimations are listed as "SI real" and "WI real".**

Summary

- gm/ID creates a connection btw the transconductance gm (a small-signal quantity) to the drain current ID (a large-signal quantity).

- The gm/ID methodology provides a unified sizing procedure for MOS devices from the ***strong to the weak inversion region***.

- The gm/ID sizing methodology applies as long as the widths are large enough so that the lateral effects can be ignored,
  - A condition that holds with most CMOS analog circuits.

- The OTA sized with this methodology results in lower current consumption with increased gain given a bandwidth.

References on gm/ID

- F. Silveira, D. Flandre, P. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," IEEE J. Solid-State Circuits, vol. 31, no. 9, Sept 1996, pp. 1314–1319.
- P. G. A. Jespers, The gm/ID Methodology, A Sizing Tool for Low-Voltage Analog CMOS Circuits, The Semi-empirical and Compact Model Approaches, Springer, Heidelberg, 2010.
- D. M. Binkley et al, "A CAD methodology for optimizing transistor current and sizing in analog CMOS design," IEEE Trans. CAD, vol. 22, no. 2, Feb. 2003, pp. 225-237.
- D. M. Binkley, Tradeoffs and Optimization in Analog CMOS Design, Wiley, Chichester, England, 2007.
- A. Girardi, F. P. Cortes, and S. Bampi, "A tool for automatic design of analog circuits based on gm/ID methodology," IEEE ISCAS, 2006.

References on EKV

- E. A. Vittoz and J. Felrath, "CMOS analog integrated circuits based on weak inversion operation," IEEE J. Solid-State Circuits, vol. 12, no. 3, pp. 224-231, June 1977.
- E. A. Vittoz, "Low-power low-voltage limitations and prospects in analog design," in Proc. Workshop Advances in Analog Circuit Design, Eindhoven, Mar. 1994.

- A good webpage on EKV by Enz: http://www.ieee.org/portal/pages/sscs/08Summer/Enz.html

Project Assignment

- Use 0.18 um (bulk or SOI) to design the OTA presented in this lecture.
- Use HSPICE level 34 model to fit the gm/ID vs $I_{□}$ curve.
- Size the transistors to achieve the maximum possible performance.
- Discuss the performance trade-offs:
  - Gain, transition frequency (f_T), PM, slew rate (SR)
  - Power and area
  - Noise