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Design Procedure for Two-Stage CMOS Transconductance Operational Amplifiers: A Tutorial

G. PALMISANO, G. PALUMBO AND S. PENNISI

Dipartimento Elettrico Elettronico e Sistemistico, Universita' di Catania, Viale Andrea Doria, 6 I-95125 Catania, Italy
Tel: ++39.095.73823.05/13/18 Fax: 39.095.330793
E-mail: gpalmisano@dees.unict.it; gpalumbo@dees.unict.it; spennisi@dees.unict.it

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Abstract. This paper deals with well-defined design criteria for two-stage CMOS transconductance operational amplifiers. A novel and simple design procedure is presented, which allows electrical parameters to be univocally related to the value of each circuit element and biasing value. Unlike previous methods, the proposed one is suited for a pencil-and-paper design and yields accurate performance optimization without introducing unnecessary circuit constraints. Bandwidth optimization strategies are also discussed. SPICE simulations based on the proposed procedures are given which closely agree the expected results.

Key Words: CMOS, amplifiers, OTAs, analog design, frequency compensation

I. Introduction

The two-stage operational transconductance amplifier (OTA) in Fig. 1 is a widely used analog building block [1–5]. Indeed, it identifies a very simple and robust topology which provides good values for most of its electrical parameters such as dc gain, output swing, linearity, CMRR, etc. Although the term OTA was originally conceived for operational transconductance amplifiers with linear transconductance (used for the implementation of continuous-time filters), for the sake of simplicity we will use the same term OTA for general operational transconductance amplifiers.

Despite its popularity, only uncomplete design procedures were proposed for this OTA which arbitrarily reduce the degree of freedom in the design equations, hence precluding the possibility to meet optimized performance [6,7]. Indeed, the approach proposed in [6] sets arbitrarily the compensation capacitor equal to the load capacitor, and that presented in [7] introduces constraints that require an onerous recursive procedure. Finally, in [8,9] optimized design is left to computer simulation by means of a symbolic analysis software.

In this paper, a well-defined procedure for two-stage OTAs is presented which allows the value of each circuit element of the amplifier (i.e., transistor aspect ratios, bias current and compensation capacitor) to be univocally related to the required amplifier performance. In such a way, OTA parameters are optimized with a straightforward pencil-and-paper analysis using accurate design equations.

The design procedure is based on the following main parameters: noise, phase margin (M_Φ), gain-bandwidth product (f_{GBW}), load capacitance (C_L), slew rate (*SR*), input common mode range (*CMR*), output swing (*OS*), and input offset voltage (due to systematic errors). When M_Φ is not given it is set to minimize settling time [10].

Important parameters such as dc gain, *CMRR* and *PSRR*, will not be used during the design steps since they depend on the output resistance of MOS transistors that is not easily modeled for a hand analysis. Such parameters greatly depend on the amplifier topology (typical dc gain and *CMRR* in a two-stage OTA are in the ranges of 60–80 dB and 70–90 dB, respectively) and can only be predicted by simulation using accurate transistor models. Of course, there are electrical pameters which can be improved with appropriate circuit arrangements. For instance, a high drive capability can be achieved by employing class AB instead of class A topologies [11–13].

The proposed procedure in its general form is described in Section II. We will use the Miller

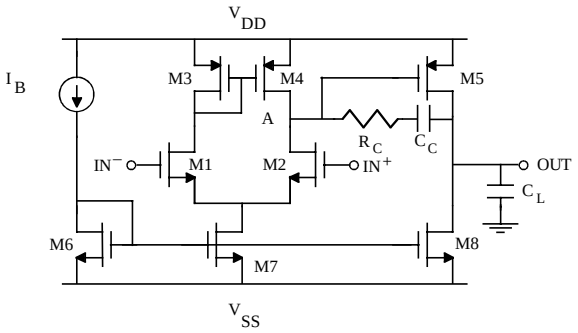


Fig. 1. Schematic of the two-stage OTA.

compensation and the nulling resistor technique for the compensation of the right half-plane zero [14].

Three other possible extensions of the general approach in Section II are discussed in Section III, which allow optimization of the gain-bandwidth product to be achieved. In these last approaches the compensation path is properly used to perform a pole-zero compensation which increases the frequency of the amplifier non-dominant pole. Unlike the general procedure, these extensions, which are optimized for gain-bandwidth product performance, need some approximations.

Design examples are provided and comparisons between simulated and expected results are also carried out.

II. Standard Design Approach

A. Description

The procedure starts from the noise requirement. Neglecting flicker noise which contributes at low frequencies, the input noise voltage spectral density of the OTA in Fig. 1 is given by

$$S_n(f) = 2 \cdot 4kT \frac{2}{3} \frac{1}{g_{m1,2}} \left[1 + \frac{g_{m3,4}}{g_{m1,2}}\right] \qquad (1)$$

where only the noise sources of the input stage have been considered. To minimize noise, we assume $g_{m3,4} < g_{m1,2}$ (which is easily met) and calculate the transconductance gain of transistors M1 and M2 from equation (1)

$$g_{m1,2} \approx \frac{16}{3} \frac{kT}{S_n(f)} \qquad (2)$$

If reduction of low frequency noise is required, flicker noise can be lowered by increasing the channel length and proportionally the channel width of M1 and M2.

Now, we are not able to determine the aspect ratio of M1 and M2, since their bias currents are not set, but the knowledge of $g_{m1,2}$ and the gain-bandwidth product requirement, allows us to draw the value of the compensation capacitor according to the following equation

$$C_C = \frac{1}{2\pi} \frac{g_{m1,2}}{f_{GBW}} \qquad (3)$$

The slew rate performance of the amplifier depends on the slews on both the output node of the differential stage and the output node of the second stage (i.e., the output of the OTA), to which we will refer as internal and external slew rate, respectively. These slew rate terms are related to the quiescent currents $I_{D1,2}$ and I_{D8} according to

$$SR_{INT} = \frac{2I_{D1,2}}{C_C} \qquad (4a)$$

$$SR_{EXT} = \frac{I_{D8} - 2I_{D1,2}}{C_L} \qquad (4b)$$

In order to satisfy slew rate performance, we have to set internal and external slew rate not lower than the target value *SR*. In a first design step we can set $SR_{INT} = SR_{EXT} = SR$ and get

$$I_{D1,2} = \frac{SR}{2} C_C \qquad (5a)$$

$$I_{D8} = SR(C_C + C_L) = 2\left(1 + \frac{C_L}{C_C}\right) I_{D1,2} \qquad (5b)$$

Remembering that $g_m = 2\sqrt{K_{n,p}(W/L)I_D}$ where $(K_{n,p} = \mu_{n,p}C_{ox}/2)$, from equation (5a) the aspect ratio of transistors M1 and M2 is

$$\left(\frac{W}{L}\right)_{1,2} = \frac{g_{m1,2}^2}{4K_N I_{D1,2}} \qquad (6)$$

For a two-stage amplifier in which the frequency behavior can well be assumed with a single non-dominant pole (i.e., a single second pole), the phase margin is expressed by

$$M_\Phi = 90^\circ - \arctan\frac{f_{GBW}}{f_{SP}} \qquad (7)$$

where, due to the pole-splitting effect, the frequency at which the second pole occurs, f_{SP}, is

$$f_{SP} = \frac{g_{m5}}{2\pi C_L} \tag{8}$$

Therefore, the transconductance gain of M5 results

$$g_{m5} = 2\pi f_{GBW} C_L \mathrm{tg}(M_\phi) \tag{9}$$

and, since $I_{D5} = I_{D8}$, its aspect ratio is

$$\left(\frac{W}{L}\right)_5 = \frac{g_{m5}^2}{4K_P I_{D8}} \tag{10}$$

Once the transconductance of transistor M5 is known, we also can find the value of the resistance R_C that compensates for the right half-plane zero caused by the forward path to the output. This resistance can be implemented with a MOS transistor in triode region and is given by

$$R_C = \frac{1}{g_{m5}} \tag{11}$$

For two-pole amplifiers, it can be useful to define the separation factor, K, between the second pole and the gain-bandwidth product

$$K = \frac{f_{SP}}{f_{GBW}} \tag{12}$$

When the amplifier phase margin is greater than 45°, f_{GBW} is equal to f_T and parameter K is equal to the tangent of the phase margin. For instance, a phase margin of 60° means a K value of about 1.7.

Using equations (3), (8) and (12), the compensation capacitor can also be expressed as

$$C_C = K\frac{g_{m1,2}}{g_{m5}} C_L \tag{13}$$

As far as transistors M3 and M4 is concerned, they contribute to the systematic offset and *CMRR*, besides affecting noise performance according to equation (1). In order to improve both offset and CMRR, accurate matching must be guaranteed by both a proper layout design and symmetrical bias conditions. This means the same drain-source voltages, other than the same aspect ratios. Consequently, we must set

$$V_{GS3} = V_{DS4} = V_{GS5} \tag{14}$$

which gives

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I_{D3,4}}{I_{D5}} \left(\frac{W}{L}\right)_5 \tag{15}$$

Starting from equation (15), we can define the length and hence the width of transistors M3 and M4 following different requirements. Setting minimal length to minimize silicon area or setting high channel length to minimize flicker noise.

Other useful relations to complete the design can be obtained by considering positive and negative *CMR* and/or *OS*, which are together linked since from equation (15) $V_{DSsat3,4} = V_{DSsat5}$ and $V_{DSsat7} = V_{DSsat8}$ (note that $V_{GS7} = V_{GS8}$). Saturation drain-source voltages have typical values in the range of 50–350 mV and are given by

$$V_{DSsat} = \sqrt{I_D/[K_{n,p}(W/L)]} \tag{16}$$

Therefore, assuming the analog ground equal to half the power supply (i.e., $V_{DD}/2$) for the positive and negative output swings we get

$$OS^+ = \frac{V_{DD}}{2} - |V_{DSsat5}| \tag{17a}$$

$$OS^- = \frac{V_{DD}}{2} - V_{DSsat8} \tag{17b}$$

and for the input common mode voltages

$$\begin{aligned} CMR^+ &= V_{DS1,2} - V_{DSsat1,2} = V_{DD} - |V_{GS3,4,5}| \\ &\quad - \left(\frac{V_{DD}}{2} - V_{GS1,2}\right) = \frac{V_{DD}}{2} - |V_{DSsat3,4,5}| \\ &\quad - |V_{TP}| + V_{TN} \end{aligned} \tag{18a}$$

$$\begin{aligned} CMR^- &= V_{DS7} - V_{DSsat7} = \frac{V_{DD}}{2} - V_{GS1,2} - V_{DSsat7,8} \\ &= \frac{V_{DD}}{2} - V_{DSsat1,2} - V_{TN} - V_{DSsat7} \end{aligned} \tag{18b}$$

Hence, in order to satisfy both the two set of conditions we have to chose

$$\begin{aligned} V_{DSsat3,4,5} &= \min\{(V_{DD}/2 - |V_{TP}| + V_{TN} \\ &\quad - CMR^+), (V_{DD}/2 - OR^+)\} \end{aligned} \tag{19a}$$

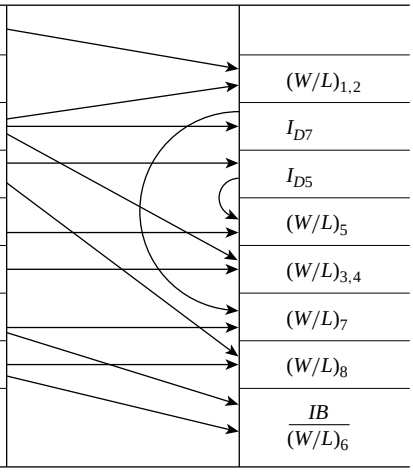
$$\begin{aligned} V_{DSsat7,8} &= \min\{(V_{DD}/2 - V_{TN} + V_{DSsat1,2} \\ &\quad - CMR^-), (V_{DD}/2 - OR^-)\} \end{aligned} \tag{19b}$$

Of course, $V_{DSsat3,4,5}$ are previously set on the base of slew rate, phase margin, gain-bandwidth, and matching requirements. Therefore, if $V_{DSsat3,4,5}$ does not meet the input and/or output positive swing requirements, a higher aspect ratio must be set for transistors M3-M5 which gives better phase margin but higher area and noise contribution.

Being currents I_{D7} and I_{D8} known, from equation (19b) we can determine the aspect ratio of transistors M7 and M8.

Table 1. Summary of the design flow.

Performance Parameters	Are Set by	Design Parameters
Noise	→	$g_{m1,2}$
f_{GBW}	→	C_C
SR_{INT}	→	$I_{D1,2}$
SR_{EXT}	→	I_{D8}
M_Φ	→	g_{m5}
Systematic offset	→	$V_{GS3} = V_{DS4} = V_{GS5}$
OS	→	V_{DSsat7}
CMR	→	V_{DSsat8}



Finally, since the drain-source saturation voltage of M6 is equal to $V_{DSsat7,8}$, we have a degree of freedom in setting current IB and the aspect ratio of M6, according to the following equation

$$I_B = \frac{(W/L)_6}{(W/L)_7} I_{D7} \tag{20}$$

The design flow, which relates the performance to the design parameters, is summarized in Table 1.

B. Simulations

In order to evaluate the accuracy of proposed procedure, the two-stage OTA in Fig. 1 has been designed by using a standard 1.2-μm CMOS technology which has the main following process parameters:

$$K_N = 30\ \mu\text{A/V}^2, \qquad K_P = 10\ \mu\text{A/V}^2,$$
$$V_{TN} = -V_{TP} = 0.75\ \text{V}.$$

The target specification is reported in the first column of Table 2. The requirement in terms of dc gain and CMRR are set on the base of the topology rather than on the design approach, as mentioned before. Furthermore, a load capacitor, C_L, equal to 4 pF has been assumed.

Using the design procedure outlined in Section II, we have determined the values of transistor aspect ratios, bias currents, compensation capacitor and nulling resistor which are shown in Table 3.

Table 2. Main electrical parameters of the OTA in Fig. 1.

Parameters	Target	Simulated
DC Gain	>60 dB	67 dB
f_{GBW}	10 MHz	12 MHz
M_Φ	60°	59°
Slew rate	10 V/μs	11.5 V/μs
Input white noise	10 nV/$\sqrt{\text{Hz}}$	13 nV/$\sqrt{\text{Hz}}$
Systematic offset	0 V	0.1 mV
OS	≥2 V	2 V
CMR	≥1.2 V	1.2 V
CMRR	>70 dB	78 dB

Table 3. Component values for the OTA in Fig. 1.

Parameters	Value	Unit
IB	18	μA
M1 M2	28/1.2	
M3 M4	17/1.2	
M5	75/1.2	
M6	7/1.2	μm/μm
M7	14/1.2	
M8	33/1.2	
C_C	3.5	pF
R_C	2.3	kΩ

In order to confirm the expected performance, SPICE simulations using LEVEL 2 models and

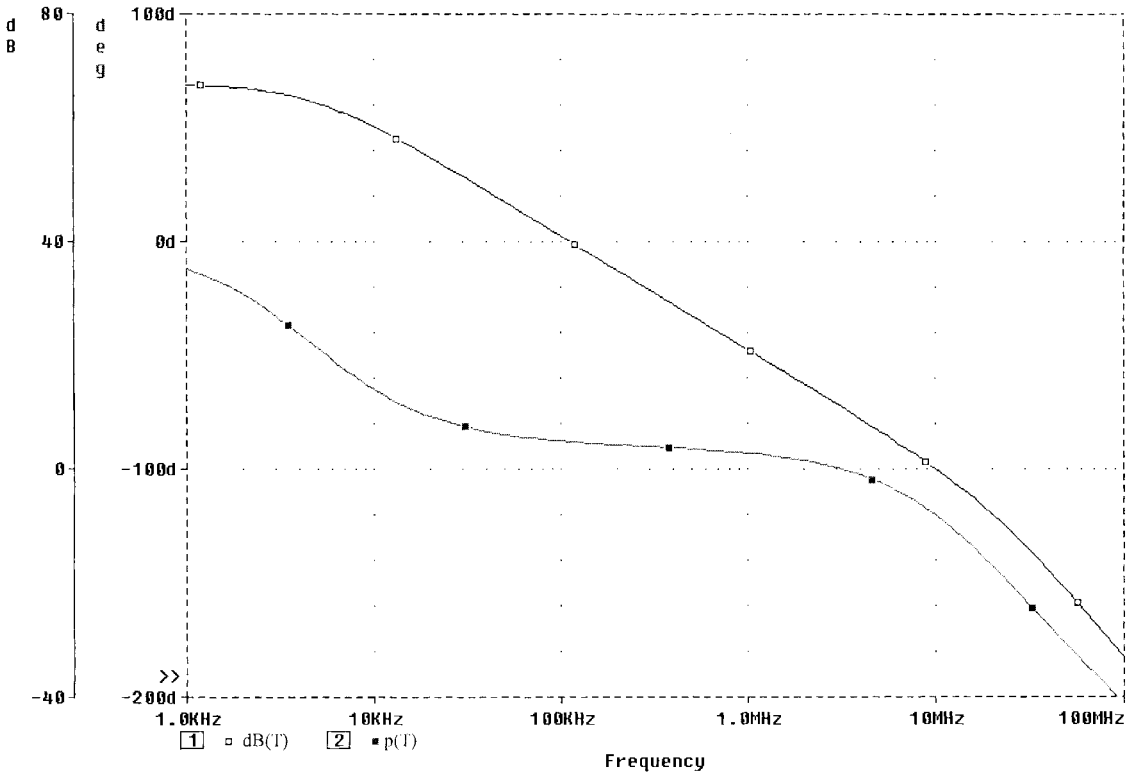


Fig. 2. Loop-gain frequency response of OTA in Fig. 1.

including device areas and perimeters have been carried out.

Fig. 2 illustrates the frequency response which shows a dc gain, a gain-bandwidth product and a phase margin of 67 dB, 9 MHz and 67°, respectively. These results are very close to the target values. A step response in unity-gain configuration is depicted in Fig. 3. The accurate agreement between the expected and simulated slew rate is apparent. Table 2 summarizes the main target and simulated parameters.

III. Optimized Design Approaches

With the previous approach, the maximum achievable gain-bandwidth is limited by the second pole, $g_{m5}/2\pi C_L$, that depends on the load capacitor C_L. Therefore, to achieve a high gain-bandwidth product a very high g_{m5} value is required. However, it has been shown that it is possible to take advantage of techniques for compensation of the right half-plane zero to obtain a better frequency response. The original of these techniques was applied to NMOS opamps [15] and then to CMOS opamps [16]. It breaks the forward path through the compensation capacitor by introducing a voltage buffer in the compensation branch. Another solution uses a current buffer to break this forward path [17]. Optimized versions of these techniques, as well as of that employing the nulling resistor, were discussed in [18–20].

In this section we will give procedures which optimize the gain-bandwidth product while keeping unchanged as much as possible all the remaining electrical parameters previously set.

A. Nulling Resistor Approach

In this approach the left half-plane zero introduced by the nulling resistor R_C in Fig. 1,

$$f_z = \frac{1}{2\pi} \frac{g_{m5}}{(g_{m5} R_C - 1)\, C_C},$$

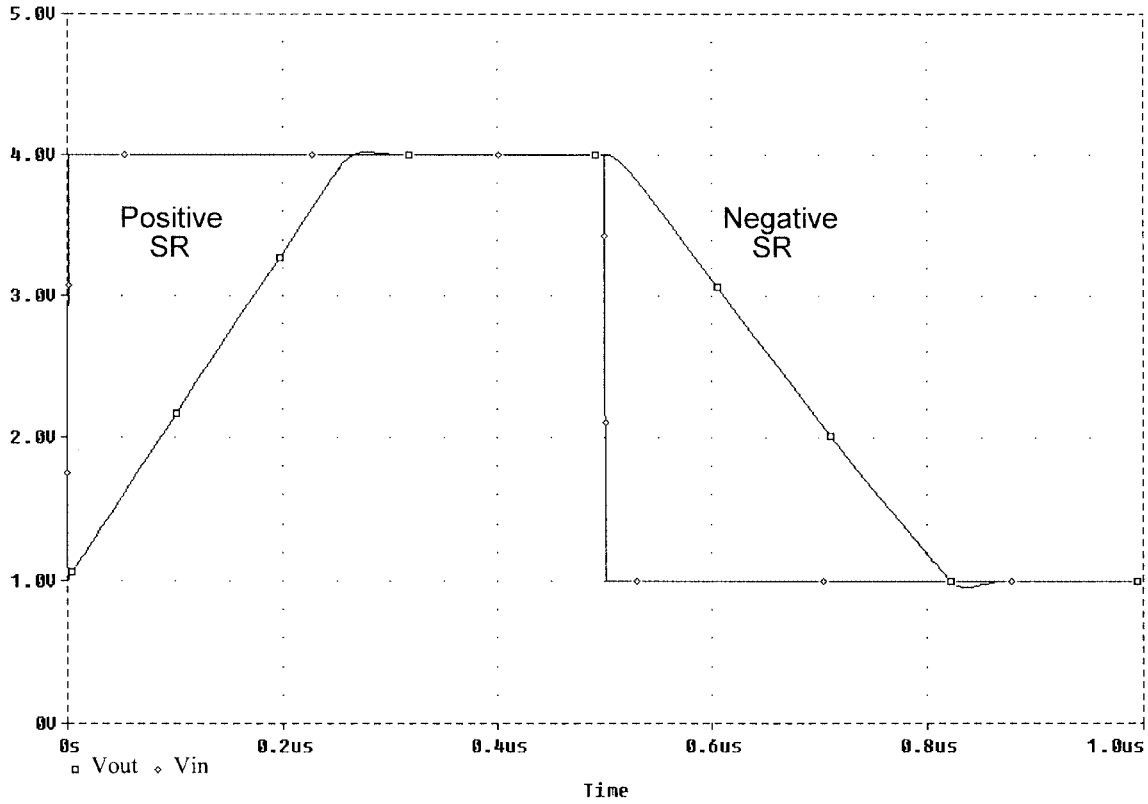


Fig. 3. Step response of the OTA in unity-gain configuration.

is exploited to compensate for the second pole given in equation (8). Therefore, the compensation sets the following condition

$$\frac{g_{m5}}{C_L} = \frac{g_{m5}}{(g_{m5}R_{CR} - 1)\,C_{CR}} \tag{21}$$

where C_{CR} and R_{CR} are the new compensation capacitor and resistor, respectively.

Once this compensation is achieved, the new second pole is [18]

$$f_{SP} = \frac{1}{2\pi\, R_{CR} C_{o1}} \tag{22}$$

where C_{o1} is the equivalent capacitance at the output of the first stage and is equal to $C_{db2} + C_{db4} + C_{gs5}$.

This second pole does not depend on the load capacitance, hence a higher gain-bandwidth product can be reached.

The final task is to choose the dominant pole (or equivalently f_{GBW}) in order to provide the desired phase margin.

Substituting equations (3) and (22) in equation (12) the new expression of K is

$$K = \frac{C_{CR}}{g_{m1,2} R_{CR} C_{o1}} \tag{23}$$

Assigned the value of K (i.e., the phase margin), from equations (21) and (23) we get C_{CR} and R_{CR}, that are

$$C_{CR} = K\frac{g_{m1,2}}{2g_{m5}}C_{o1}\left(1 + \sqrt{1 + 4\frac{g_{m5}}{g_{m1,2}}\frac{C_L}{C_{o1}}}\right) \cong K\sqrt{\frac{g_{m1,2}}{g_{m5}}C_{o1}C_L} \tag{24a}$$

$$R_{CR} = \frac{1}{2g_{m5}}\left(1 + \sqrt{1 + 4\frac{g_{m5}C_L}{K g_{m1,2}C_{o1}}}\right) \cong \sqrt{\frac{C_L}{K g_{m1,2} g_{m5} C_{o1}}} \tag{24b}$$

where the approximations hold for C_L greater than C_{o1}.

Equation (24a) shows that the compensation capacitor is now approximately proportional to the geometric media of C_{o1} and C_L and hence is lower than that in equation (13). Therefore, the optimized approach with nulling resistor provides a higher gain-bandwidth product.

B. *Voltage Buffer Approach*

Let us consider the compensation technique which uses a voltage buffer to break the forward path through the compensation branch. Usually, the simple common drain in Fig. 4 is employed and connected between nodes A and OUT in Fig. 1. Taking into account for the finite output resistance of the buffer which is about equal to $1/g_{m9V}$, the compensation branch introduces a left half-plane zero at $f_z = g_{m9V}/2\pi C_{CV}$.

Therefore, a pole-zero compensation with the original second pole is achieved by setting

$$\frac{g_{m5}}{C_L} = \frac{g_{m9V}}{C_{CV}} \tag{25}$$

The compensation is highly accurate since it only depends on matching tolerances between transconductances and capacitors. Using this technique, the new second pole is

$$f_{sp} = \frac{g_{m9V}}{2\pi C'_{o1}} \tag{26}$$

where $C'_{o1} \cong C_{o1} + C_{gs9V}$ is the equivalent capacitance at the output of the first stage. The separation factor is given by

$$K = \frac{g_{m9V}}{g_{m1,2}} \frac{C_{CV}}{C'_{o1}} \tag{27}$$

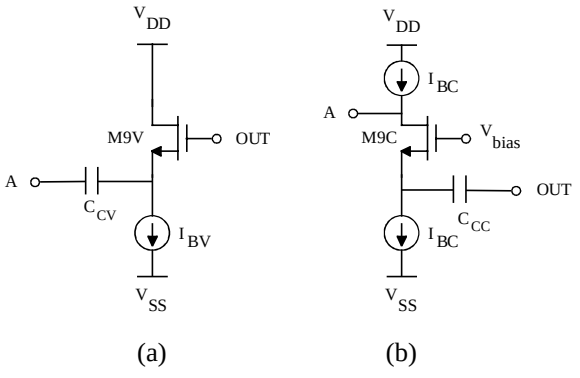


Fig. 4. Voltage buffer (a) and current buffer (b) compensation blocks.

Since the actual value of C'_{o1} is unknown (it depends on the aspect ratio of transistor M9V that has to be still computed), evaluation of the exact solution for g_{m9V} and C_{CV} needs an iterative method. However, to provide a high second pole a small geometrical dimension for M9V has to be set. Hence, we can neglect C_{gs9V} with respect to C_{o1} and solve equations (25) and (27) for C_{CV} and g_{m9V}. It results

$$C_{CV} \cong \sqrt{K \frac{g_{m1,2}}{g_{m5}} C_{o1} C_L} \tag{28a}$$

$$g_{m9V} \cong \sqrt{K g_{m5} g_{m1,2} \frac{C_{o1}}{C_L}} \tag{28b}$$

It is apparent from equations (24a) and (28a), that the approaches based on nulling resistor and voltage buffer give the same compensation capacitor and hence the same gain-bandwidth product. However, a voltage buffer in the compensation branch greatly reduces the output swing preventing its use in many practical cases.

C. *Current Buffer Approach*

Let us consider the compensation technique which uses a current buffer to break the forward path through the compensation branch. At this purpose, the common gate in Fig. 4b can be used which is connected between nodes A and OUT in Fig. 1. In this case the open-loop gain is characterized by a dominant pole, a zero (given by $g_{m9C}/2\pi C_{CC}$), and two complex and conjugate poles. A detailed treatment of this subject can be found in [20] where it is demonstrated that the gain-bandwidth product optimization is achieved by setting

$$g_{m9C} = 2g_{m1,2} \tag{29a}$$

and

$$C_{CC} \cong \sqrt{\frac{g_{m12}}{g_{m5}} \left(\frac{2K-1}{2+K} + \frac{1}{2} \right) C_L C_{o1}} \tag{29b}$$

Assuming similar electrical parameters, phase margin and load capacitance, capacitance C_{CC} is slightly lower than capacitance C_{CV} and hence the gain-bandwidth product in this last case is the highest among the optimized approaches.

Moreover, the optimization using current buffer preserves the original output swing. Finally, a better implementation of this approach can be achieved by

using a cascode differential stage instead of a simple differential stage and taking advantage one of the two common gates.

D. Final Remarks

The frequency limitation of the current mirror M3-M4, which performs the differential to single ended conversion [21–22], introduces a pole-zero doublet with the zero higher than the pole by an octave.

The doublet can be neglected in the traditional design described in Section II, but must be considered in the optimized approaches due to the high value of the gain-bandwidth product.

Since the pole and zero are close one to each other, the doublet does not appreciably modify the transition frequency but it can greatly affect the phase margin. From a design point of view, it can be shown that taking into account the pole-zero means a larger compensation capacitor which in turn leads to a smaller gain-bandwidth product [23–24]. The new gain-bandwidth product, f_{NGBW}, is approximately given by [23–24]

$$f_{NGBW} \cong \frac{2 f_{sp} f_d^2}{K f_d (2 f_d + f_{sp})} \tag{30}$$

where f_d is the pole frequency of the doublet and is equal to $g_{m3,4}/2\pi 2C_{gs4}$.

Therefore, the new compensation capacitor, C_{NC}, which provides the desired phase margin is given by

$$C_{NC} = \frac{f_{GBW}}{f_{NGBW}} C_C \tag{31}$$

E. Simulations

We have worked out three design examples to validate the optimized approaches. The same data of the numeric example in Section II have been used, setting the value of K to 2 (i.e., a phase margin of 63°). From equations (24), (28) and (29), with $C_{o1} = 168$ fF given from the previous design, the following values for the compensation network components are obtained

$$C_{CR} = 0.7 \text{ pF and } R_{CR} = 10.8 \text{ k}\Omega$$
$$C_{CV} = 0.7 \text{ pF and } g_{m9V} = 1 \times 10^{-4} \text{ A/V}$$
$$C_{CC} = 0.6 \text{ pF and } g_{m9C} = 4.3 \times 10^{-4} \text{ A/V}$$

Table 4. Component values for the voltage and current buffer.

Parameters	Value	Unit
I_{BV}	18	μA
M9V	7/1.2	μm/μm
I_{BC}	36	μA
M9C	50/1.2	μm/μm

Table 5. Calculated and simulated parameters for the optimized designs.

Optimum	Expected		Simulated[a]		Simulated[b]	
Compensation Method	f_{GBW} (MHz)	M_Φ (deg.)	f_{GBW} (MHz)	M_Φ (deg.)	f_{GBW} (MHz)	M_Φ (deg.)
Resistance	32	63	41	51	38	57.5
Voltage buffer	39	63	38	48	36.5	54
Current buffer	41	63	47.5	42	44	56

[a]Without taking into account the pole-zero doublet.
[b]Taking into account the pole-zero doublet.

which refer to the nulling resistor, the voltage buffer and the current buffer compensation approaches, respectively.

The amplifiers have been designed using these values, the aspect ratios of transistors M1–M8 and current IB in Table 3, and the component values for the voltage and current buffer in Table 4. Real active loads have been used for the current generators in Fig. 4. The expected and simulated gain-bandwidth and phase margin are reported in columns 1 and 2 of Table 5, respectively. The simulated values show a phase margin which is in all cases lower than the expected one and differs by about 15 degrees for the voltage buffer. This deviation is mainly caused by the pole-zero doublet that is not taken into account in the calculated performance. Actually, the doublet pole frequency is around 350 MHz in our designs and affects mainly the phase margin as mentioned before.

Remembering the remarks in subsection *D*, we can account for the pole-zero doublet by considering a lower gain-bandwidth product and hence a new compensation capacitance, leaving unchanged the phase margin (see equations (28) and (29)). The new compensation capacitances are nearly equal to 0.9 pF for the three designs. After this optimization, the simulated results are shown in the third column of Table 5 which good agree the expected ones.

Of course, gain-bandwidth products as high as 40 MHz are the ultimate performance for a two-stage amplifier with the selected 1.2 μm-CMOS process. At

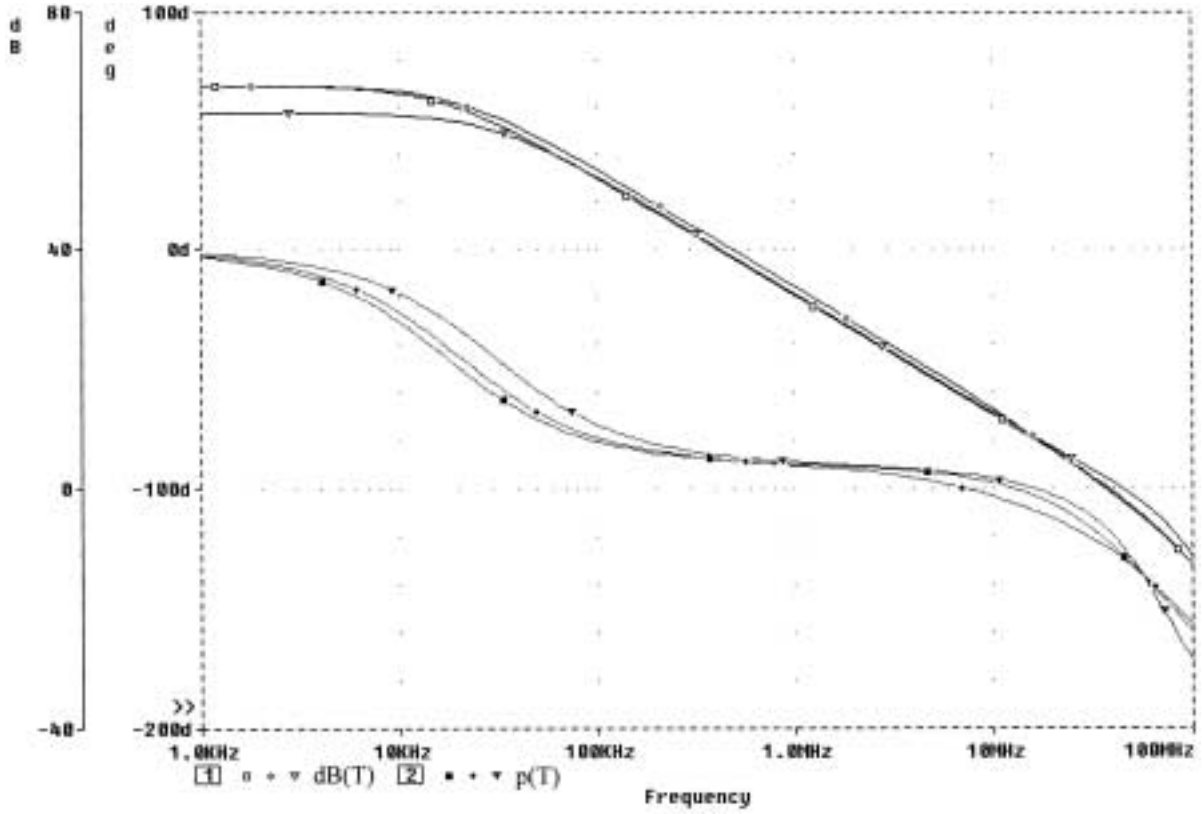


Fig. 5. Frequency responses of the loop-gain for the optimized compensation techniques: (/) nulling resistor, (◇) voltage buffer and (∇) current buffer.

this frequency we should consider second-order effects such as the pole-zero doublet due to the source-coupled pair and mainly the uncompensated half-plane zero due to the gate-drain capacitance of transistor M5. However, the last results in Table 5 are, without any doubt, an optimum starting point for a further optimization.

Fig. 5 illustrates the frequency response of the three amplifiers. The loss of 4.5 dB in the gain of the amplifier compensated with the current buffer is due to the finite output resistance of the upper current generator in Fig. 4b. The original gain can be restored by adopting the alternative implementation suggested in subsection *C*.

IV. Conclusions

A general approach for the design of two-stage CMOS transconductance amplifiers has been presented. It is based on first-order transistor models and provides simple equations for an accurate pencil-and-paper standard design. Despite its simplicity, the proposed strategy allows calculated performance to be closely in agreement with the simulated one.

Optimized designs for high gain-bandwidth product are also discussed which use typical frequency compensation techniques.

The proposed approach is a valid aid for analog designers and, especially for the standard design procedure, it can well be integrated into an analog knowledge-based CAD tool.

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Palmisano was born in Lampedusa, Italy, in 1956. He graduated in 1982 with a degree in Electronics Engineering at the University of Pavia, Italy. From 1983 to 1991, he research there, as researcher, at the Department of Electronics, in the field of CMOS and BiCMOS analog integrated circuits. In 1992, he was visiting professor at UAM (Universidad Autonoma Metropolitana) in Mexico City where he held a course on microelectronics for the doctoral students. In 1993 and 2000, he joined the Faculty of Engineering at the University of Catania as Associate Professor and Full Professor, respectively, teaching Microelectronics.

Since 1995, he has been a consultant for STMicroelectronics in the design of RF integrated circuits for portable communications equipment.

He has designed several innovative analog circuits such as operational amplifiers, switched-capacitor filters, A/D and D/A converters, within the framework of national and European research projects, as well as several integrated circuits for both the base-band and the RF front-end of mobile communications systems, within research collaborations with electronics industries.

He is co-author of more than 100 papers in international journals and conference proceedings, a book on current operational amplifiers, and several international patents.

His current research interests include low-voltage amplifiers and RF integrated circuits.

Palumbo was born in Catania, Italy, in 1964. Since the middle of 1987 he worked at the Instituto Elettrico e Elettronico" of the University of Catania, towards its laurea degree whose main topic was the design of electronic circuits by means expert systems. He received the laurea degree in Electrical Engineering and the Ph.D. degree from the *University of Catania* in 1988 and 1993, respectively. In 1989 he was awarded with a grant by AEI of Catania. In 1993, he conducted the course on Electronic Devices for diploma degree in Electronics Engineering, and now he teaches a course on *Electronics for Digital Systems* and a *first course of Electronics*. In 1994, he joined the *Department of Electrical Electronics and System* (DEES) at the *University of Catania* as a researcher, and in 1997 he became an associate professor. Now he is a full professor at the same department.

His primary research interest was analog circuits with particular emphasis on feedback circuits, compensation techniques, current-mode approach, low-voltage circuits. Recently, his research involves digital circuits with emphasis on high performance digital circuit. In these fields he is developing some the research activities in collaboration with *ST microelectronics* of Catania.

He is co-author of the book CMOS Current Amplifiers, Kluwer Academic Publishers, 1999. Moreover, he is author or co-author of more than 130 scientific papers on referred international journals and conferences. He is serving as an *Associated Editor* of the *IEEE Transaction on Circuits and Systems* part I. Prof. Palumbo is an IEEE *Senior Member*.

Salvatore Pennisi was born in Catania, Italy, in 1965. He received the laurea degree in Electronics Engineering in 1992, and in 1997 the Ph.D. degree in Electrical Engineering, both from the University of Catania. In 1996 he joined the Faculty of Engineering, University of Catania, as a researcher, and from 1999 he teaches a course on electronics. His primary research interests include CMOS analog design with emphasis on current-mode techniques. In this field he developed various innovative building blocks and unconventional architectures of operational amplifiers. More recently, his research activity involves low-voltage/low-power circuits and multi-stage amplifiers (with related optimized compensation techniques), and IF CMOS blocks. Dr. Pennisi is co-author of more than 50 publications on international journals and conferences, of a scientific monograph titled CMOS Current Amplifiers (Kluwer Academic Publishers, 1999), and has contributed to the Wiley Encyclopedia of Electrical and Electronics Engineering (Wiley & Sons, 1999).