# Hierarchical Exact Symbolic Analysis of Large Analog Integrated Circuits By Symbolic Stamps

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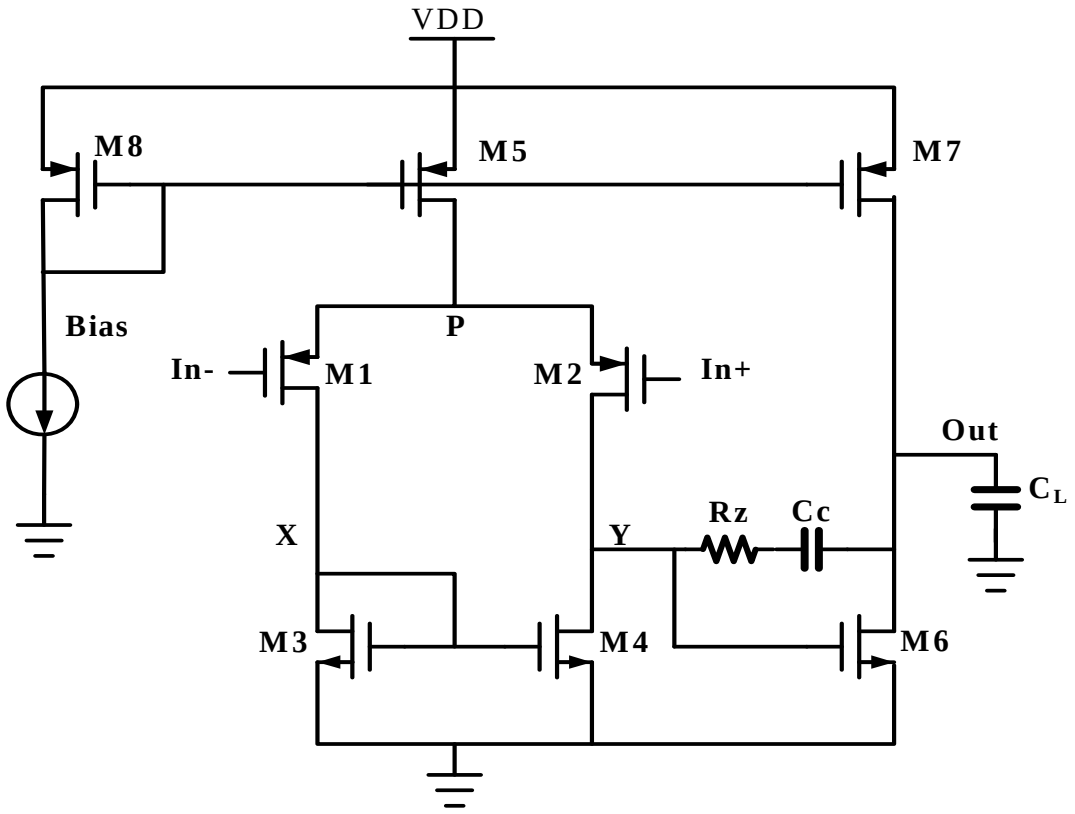
# Contents

- Motivation and Background
- The Idea of “Symbolic Stamp”
- Implementation
- Experimental Results
- Conclusion

# Motivation

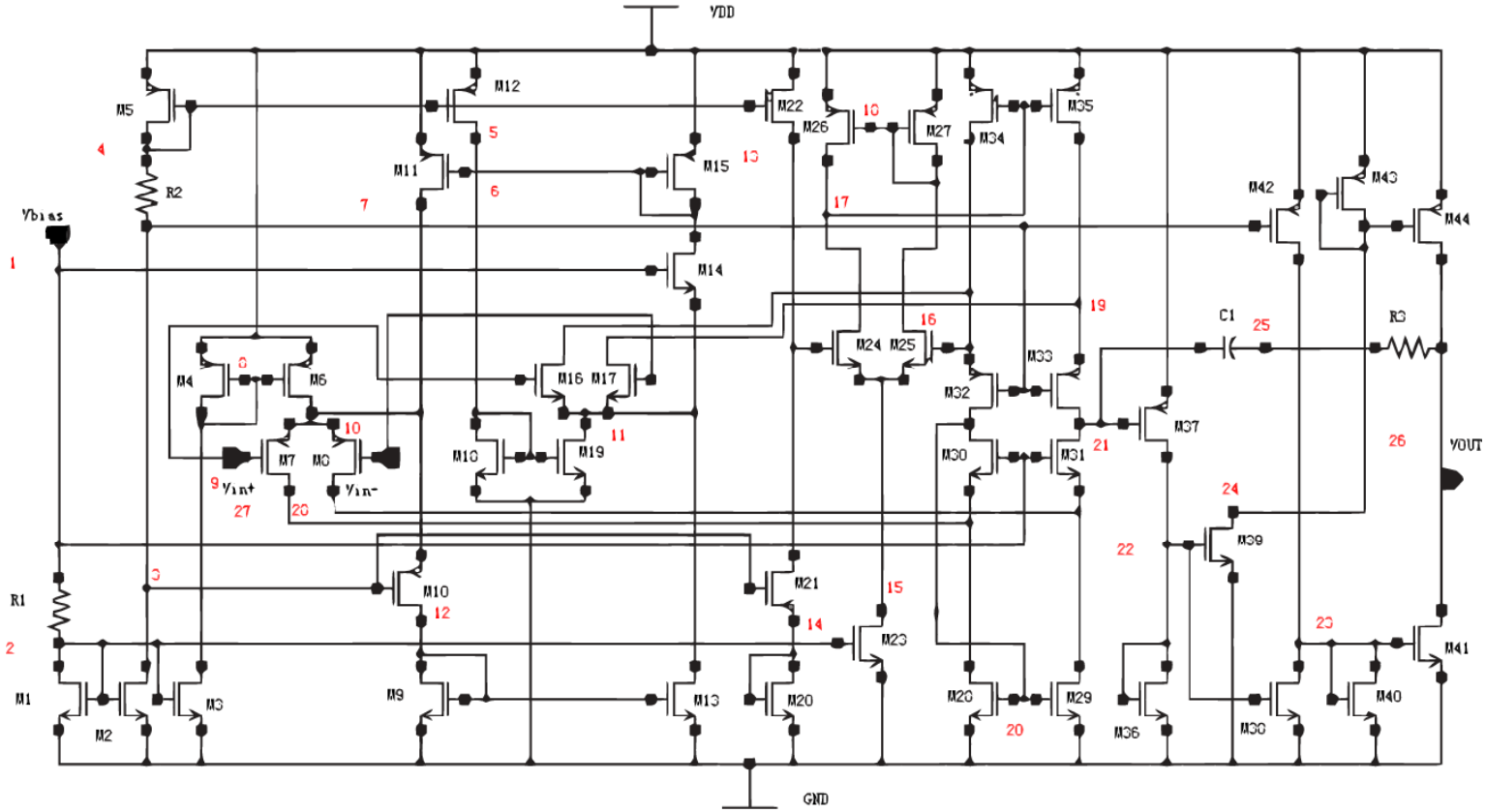
# Small Case

- Can be handled by existing **exact** symbolic analysis method



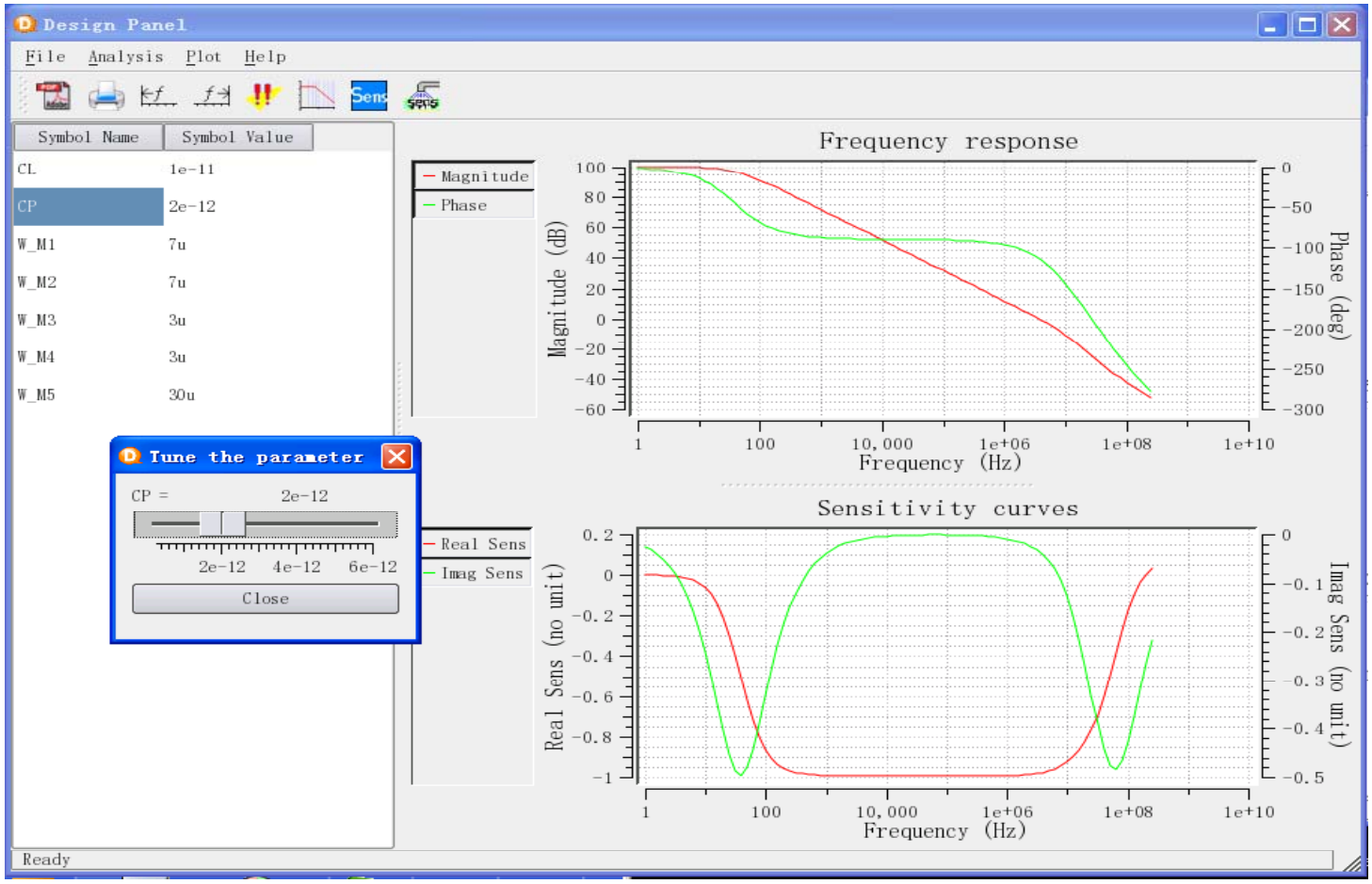
# Large Case

- **Cannot** be handled by existing **exact** symbolic analysis method



# Possible Application

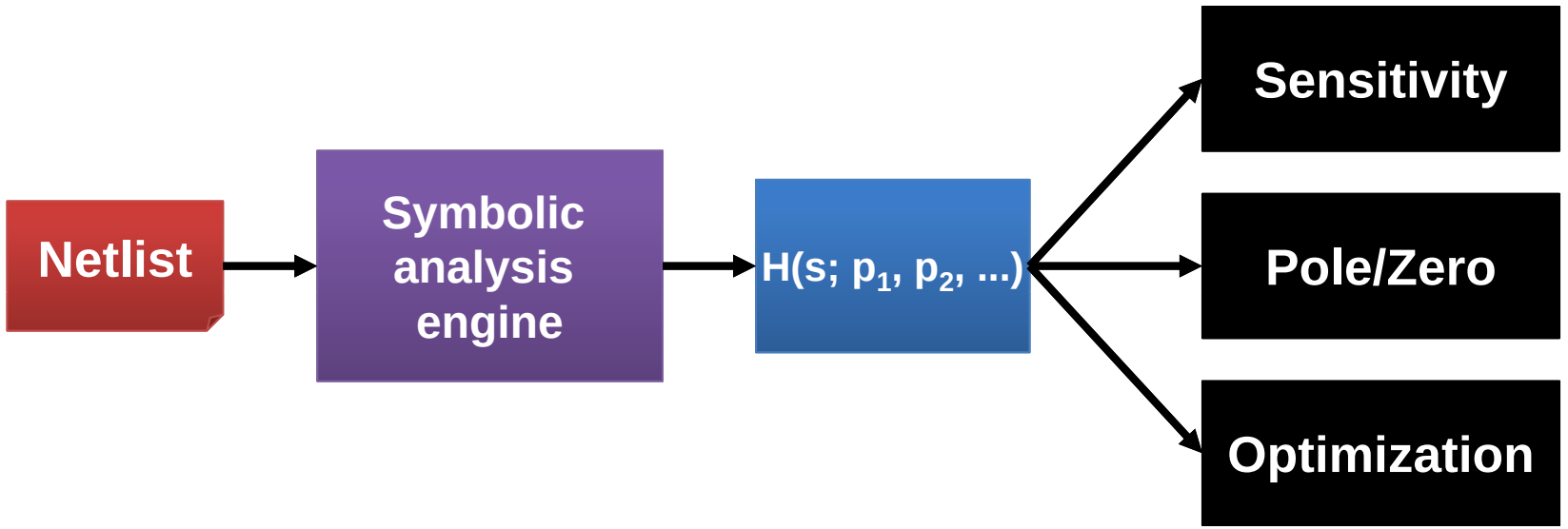
- Graphical Sensitivity Analysis[16]



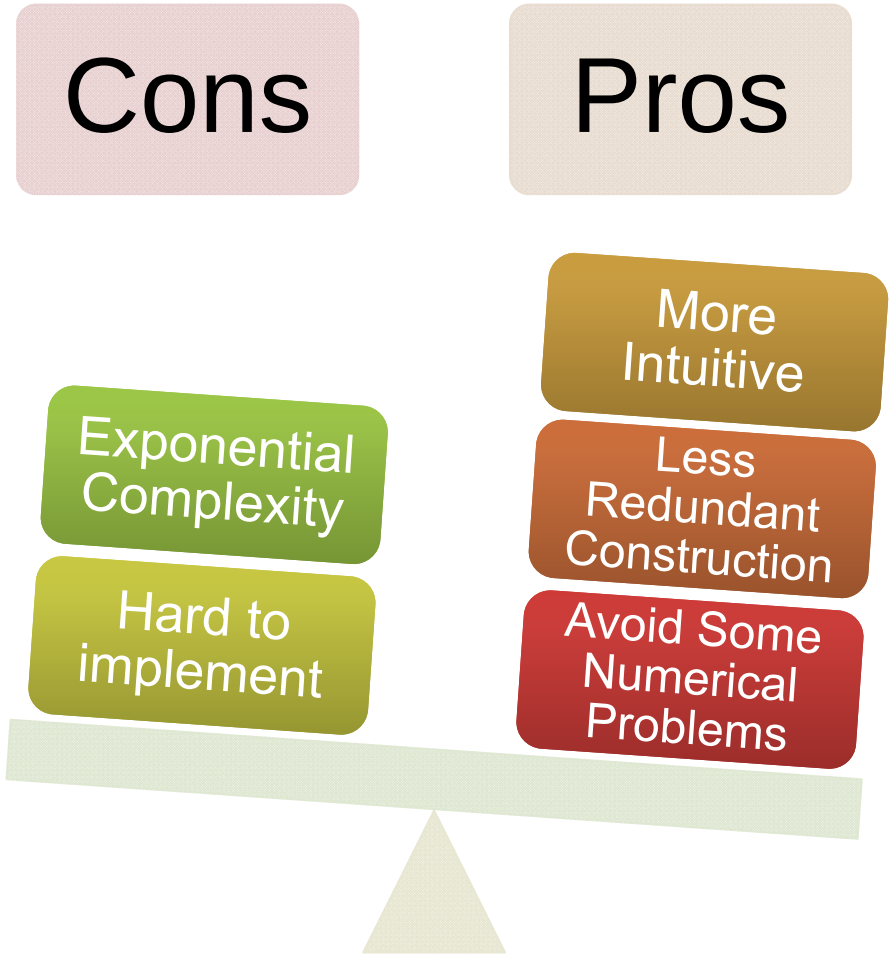

[16] D. Ma, G. Shi, and A. Lee, “A design platform for analog device size sensitivity analysis and visualization,” in *Proc. Asia Pacific Conference on Circuits and Systems (APCCAS)*, Malaysia, Dec. 2010

# Motivation: Exact Analysis

- Many circuit characteristics (sensitivity, poles, zeros) require an “exact” symbolic expression of H(s).
- Exact symbolic analysis of large analog circuits (20 ~50 MOSFETs) is not easy.

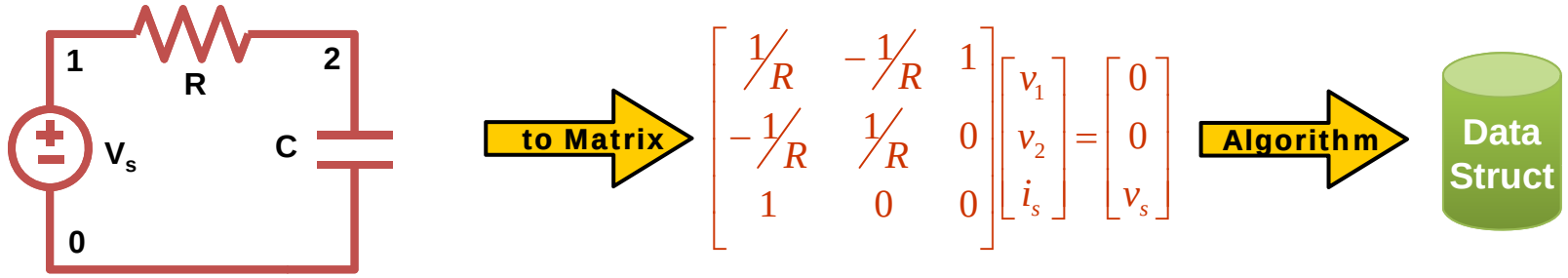


# Symbolic Analysis

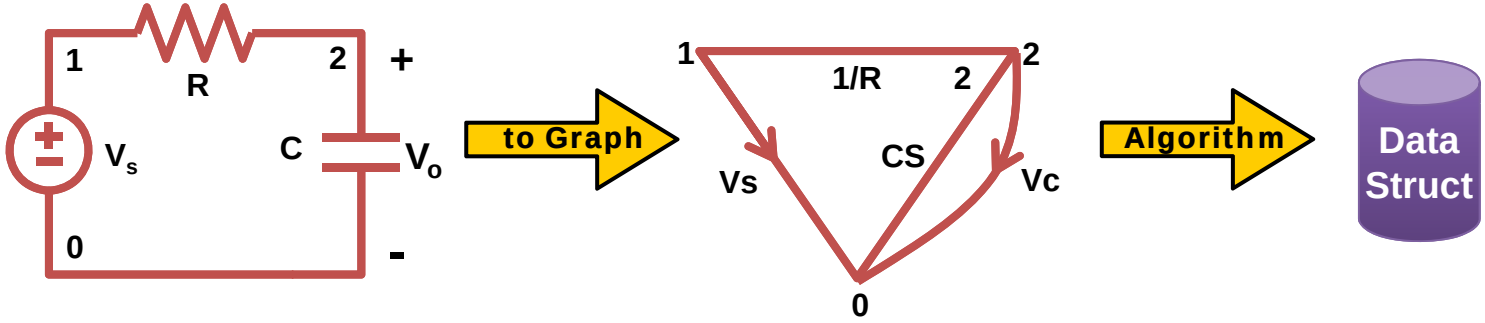


# Representative Methods

- Algebraic Methods – Determinant Decision Diagram[15]




- Graph-based Methods – Graph Pair Decision Diagram[16]

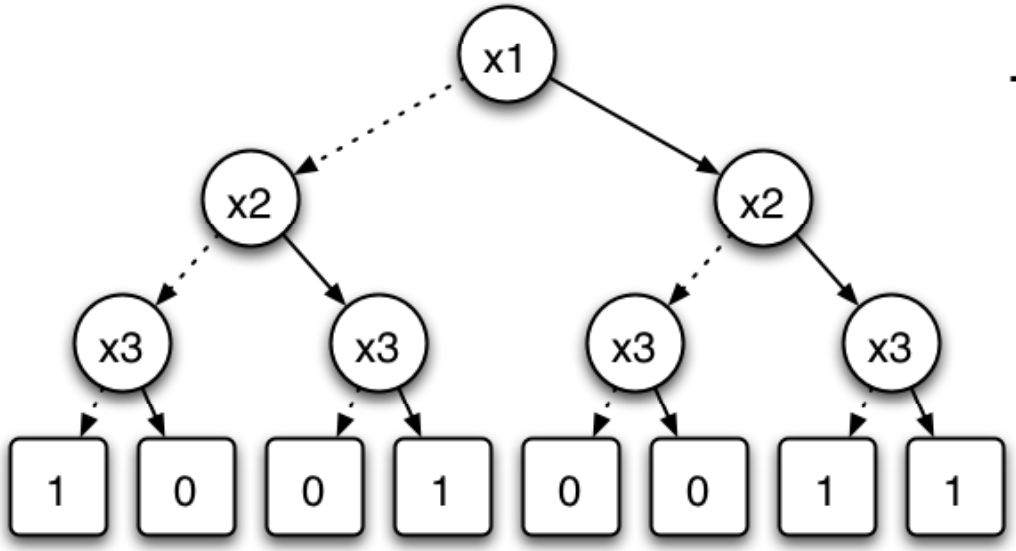



[15] C.-J. Shi and X.-D. Tan, "Canonical symbolic analysis of large analog circuits with determinant decision diagrams," *IEEE Trans. on Computer-Aided Design*, vol. 19, no. 1, pp. 1-18, Jan., 2000.

[16] G. Shi, W. Chen and C.-J. Shi, "A Graph Reduction Approach to Symbolic Circuit Analysis," in Proc. Asia and South-Pacific Design Automation Conference (ASPDAC), Yokohama, Japan, pp. 197-202, Jan., 2007.

# From Binary Tree to BDD

- Binary Tree



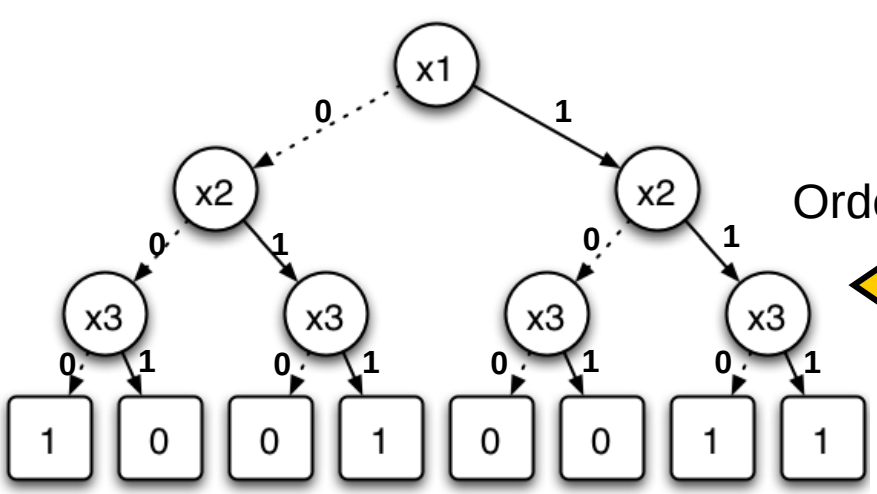

| x1 | x2 | x3 | *f* |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

$$f(x_1, x_2, x_3) = \overline{x}_1\overline{x}_2\overline{x}_3 + \overline{x}_1 x_2 x_3 + x_1 x_2 x_3 + x_1 x_2 \overline{x}_3$$

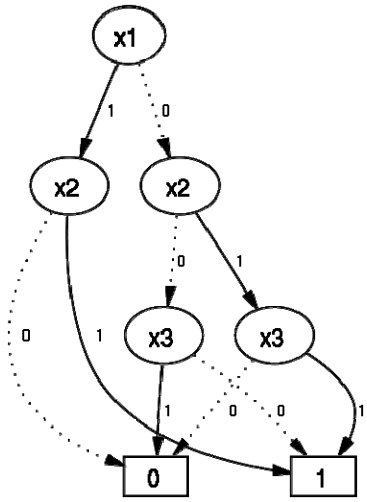
[14] R. E. Bryant, “Graph-based algorithms for Boolean function manipulation,” IEEE Trans. Comput., vol. C-37, pp. 677-691, Aug., 1986.

# Reduced Ordered BDD

Canonical and Compact!




Order: x1 > x2 > x3




$$f(x_1, x_2, x_3) = \overline{x}_1\overline{x}_2\overline{x}_3 + \overline{x}_1 x_2 x_3 + x_1 x_2 x_3 + x_1 x_2 \overline{x}_3$$

$$f(x_1, x_2, x_3) = \overline{x}_1\overline{x}_2\overline{x}_3 + x_1 x_2 + x_2 x_3$$

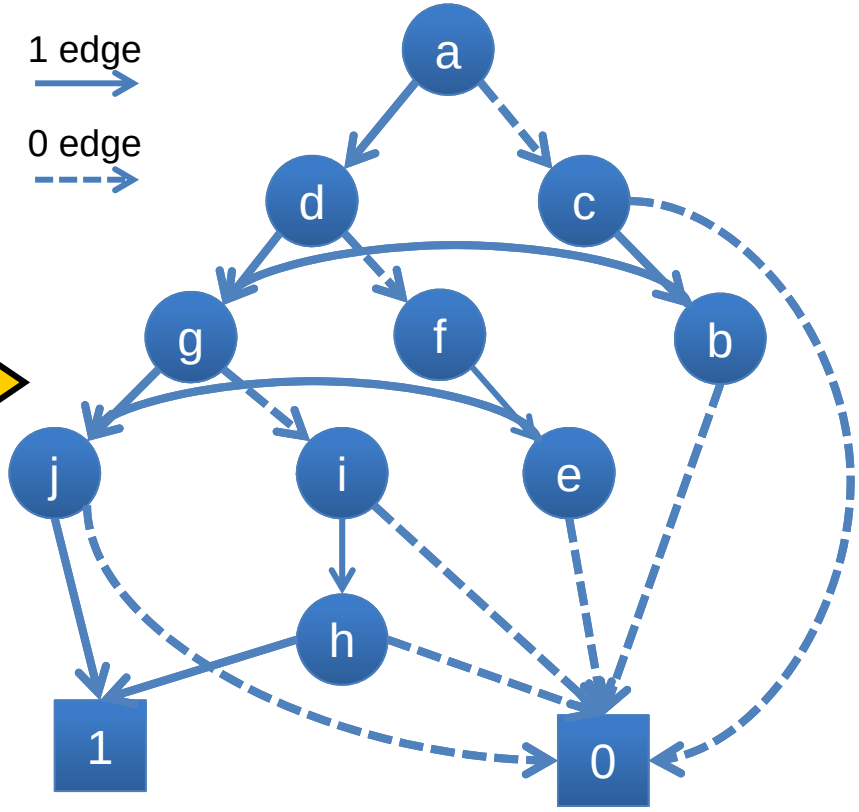

[14] R. E. Bryant, “Graph-based algorithms for Boolean function manipulation,” IEEE Trans. Comput., vol. C-37, pp. 677-691, Aug., 1986.

# Determinant Decision Diagram

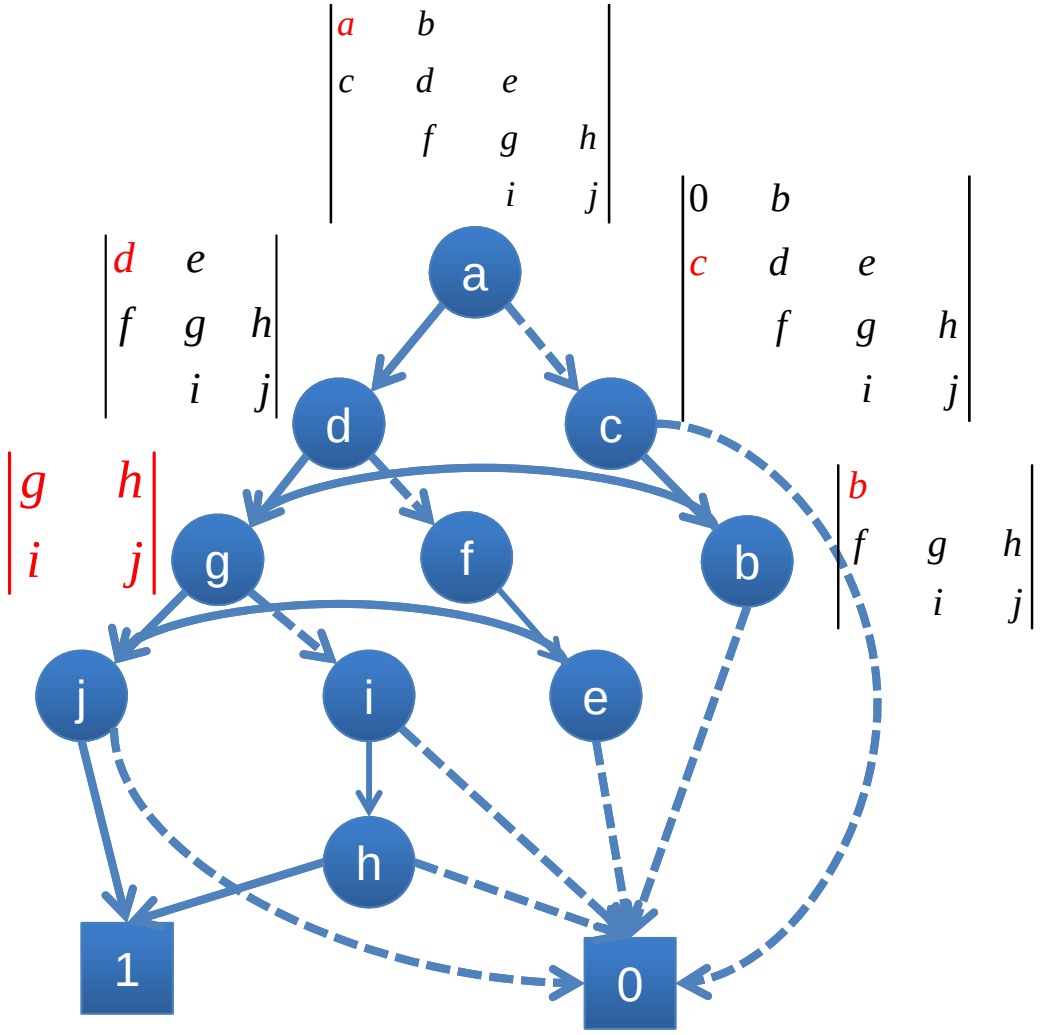
- Represent a determinant by BDD
- Treat *Laplace Expansion* as binary decisions

$$\det(A) = \begin{vmatrix} a & b & & \\ c & d & e & \\ & f & g & h \\ & & i & j \end{vmatrix}$$

$$= adgj - adhi - aefj - bcgj + cbih$$



# Minor Sharing[25]

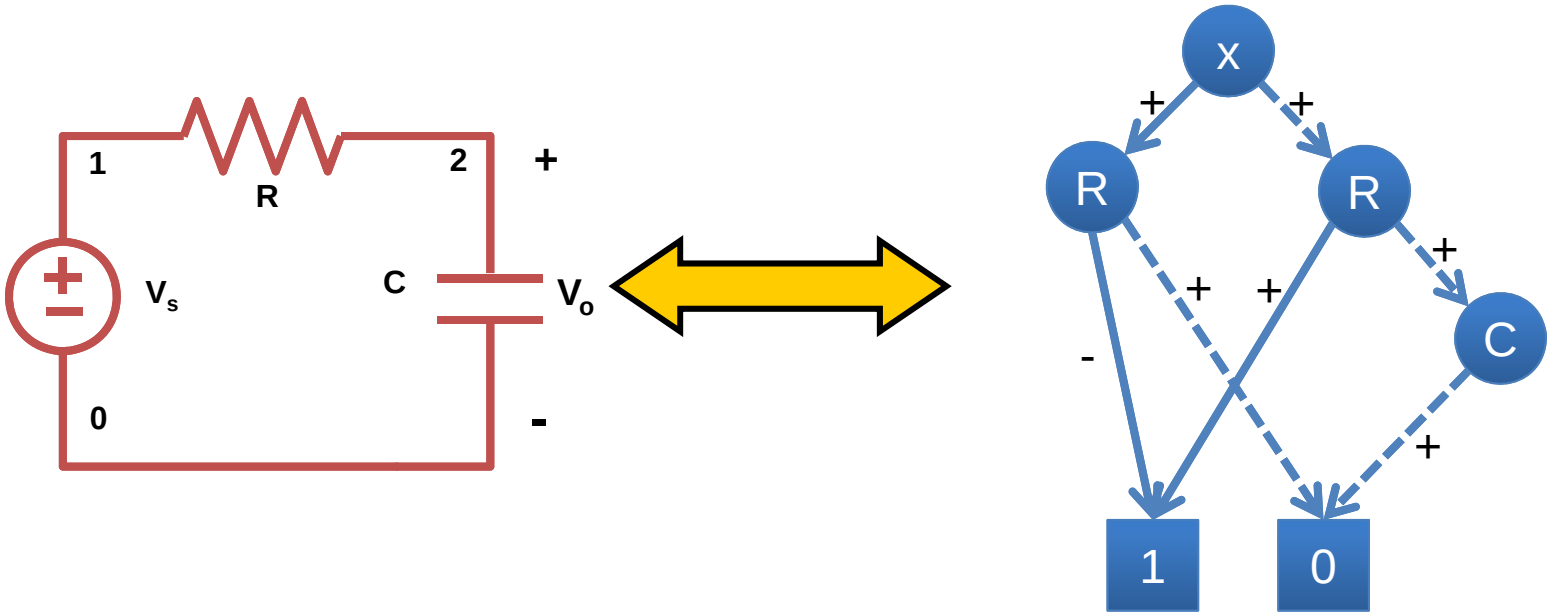




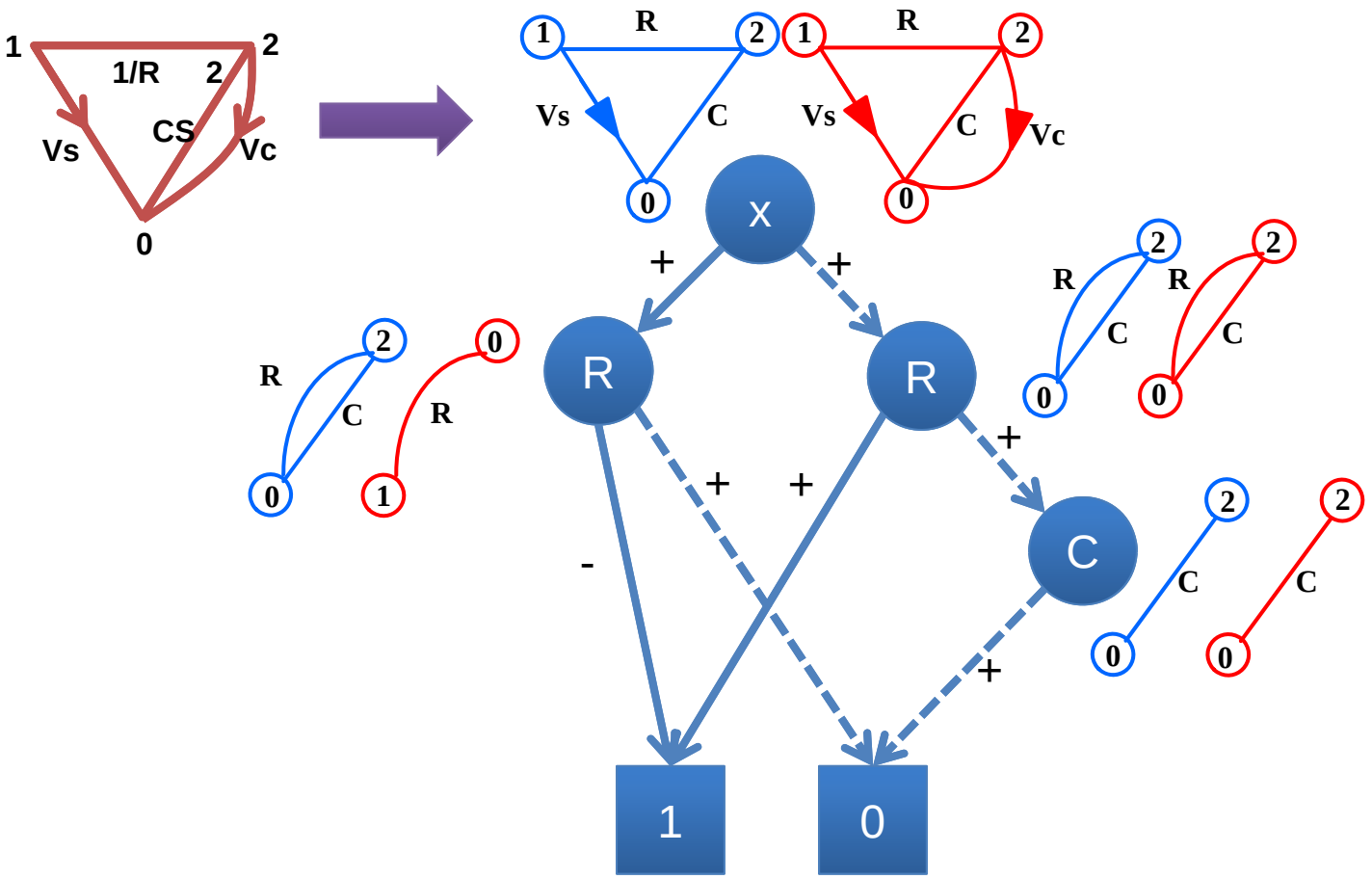

[25] G. Shi, “A simple implementation of determinant decision diagram,” in *Proc. International Conf. on Computer-Aided Design (ICCAD)*, San Jose, CA, USA, Nov. 2010.

# Graph Pair Reduction Diagram

- Represent the transfer function by BDD
- Treat *Spanning-Tree Enumeration* as binary decisions



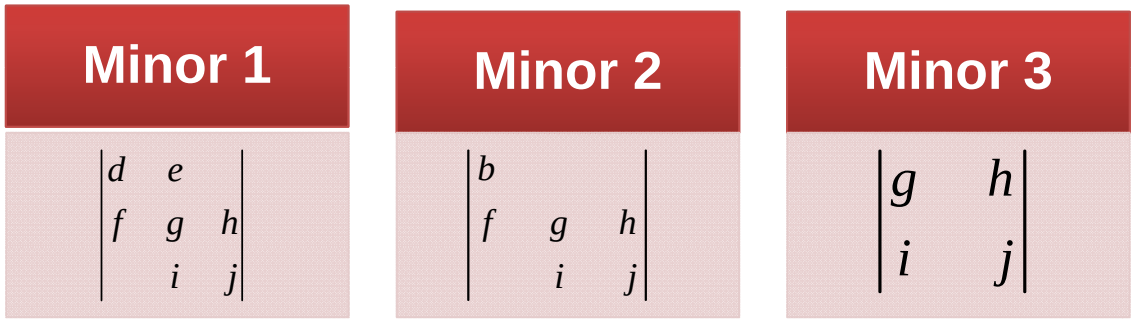
# Graph Pair Sharing[16]



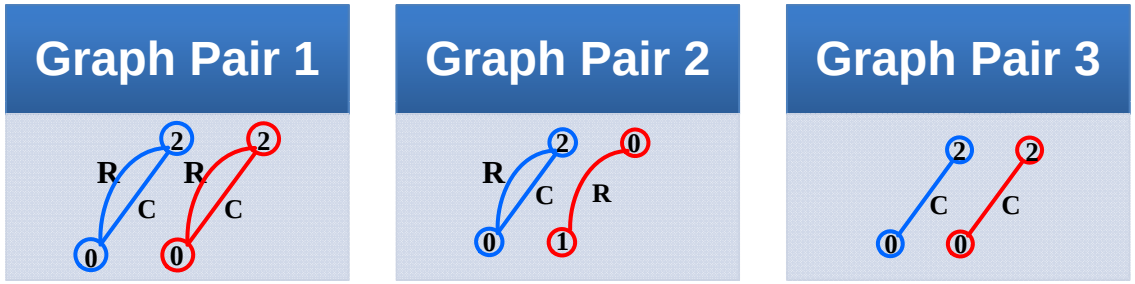

[16] G. Shi, W. Chen, and C.-J. R. Shi, “A graph reduction approach to symbolic circuit analysis,” in *Proc. Asia South-Pacific Design Automation Conference (ASPDAC)*, Yokohama, Japan, Jan. 2007, pp. 197–202.

# Hash Mechanisms

- DDD – By Hashing Minors

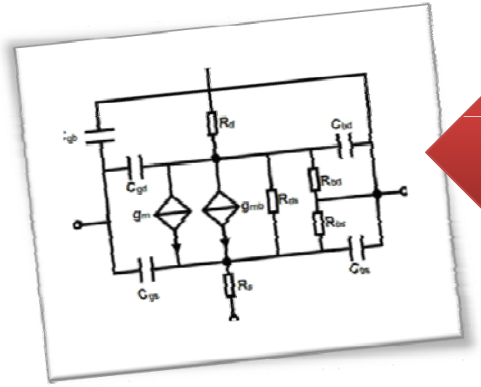


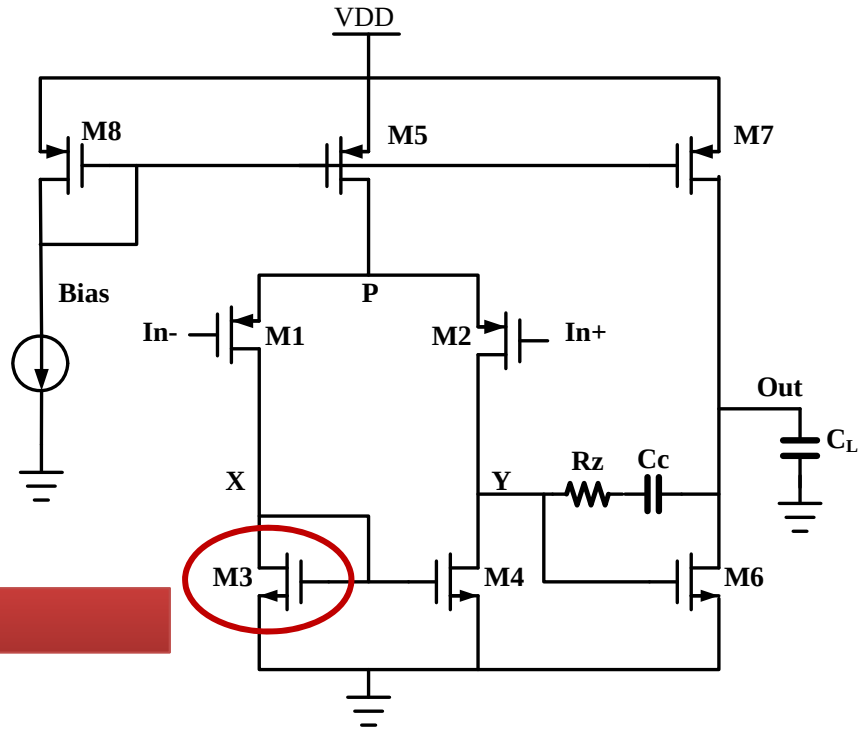

- GPDD – By Hashing subgraphs



# Idea of “Symbolic Stamp”

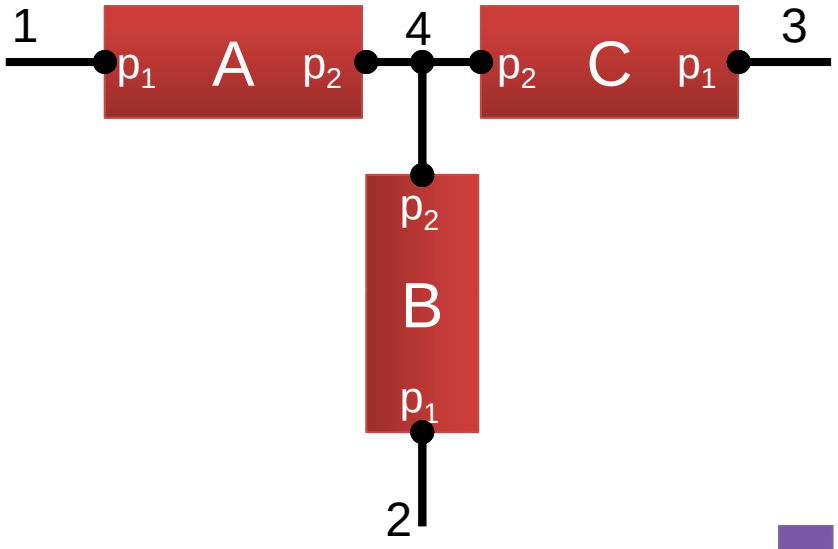
# Symbolic Stamp






- **All MOSFETs use the same small-signal model!**
- **Circuits are naturally hierarchical!**

# Assembling Symbolic Stamps

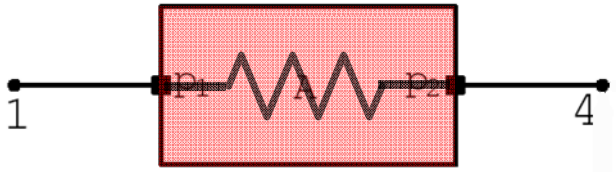



$$
\begin{array}{c} \\ n1 \\ n2 \\ n3 \\ n4 \end{array}
\begin{array}{c}
\begin{array}{cccc} n1 & n2 & n3 & n4 \end{array} \\
\begin{bmatrix}
y_{11}^{A} & & & y_{12}^{A} \\
 & y_{11}^{B} & & y_{12}^{B} \\
 & & y_{11}^{C} & y_{12}^{C} \\
y_{21}^{A} & y_{21}^{B} & y_{21}^{C} & y_{22}^{A} + y_{22}^{B} + y_{22}^{C}
\end{bmatrix}
\end{array}
$$

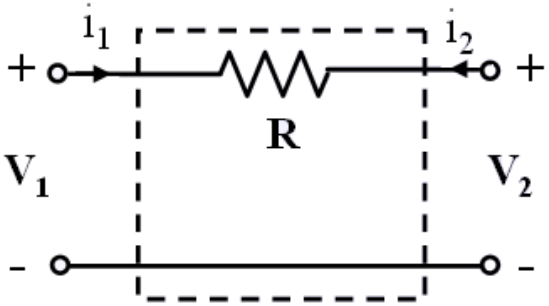
**DDD Routine**

# Procedure

## 2. Build symbolic stamp of each sub-block



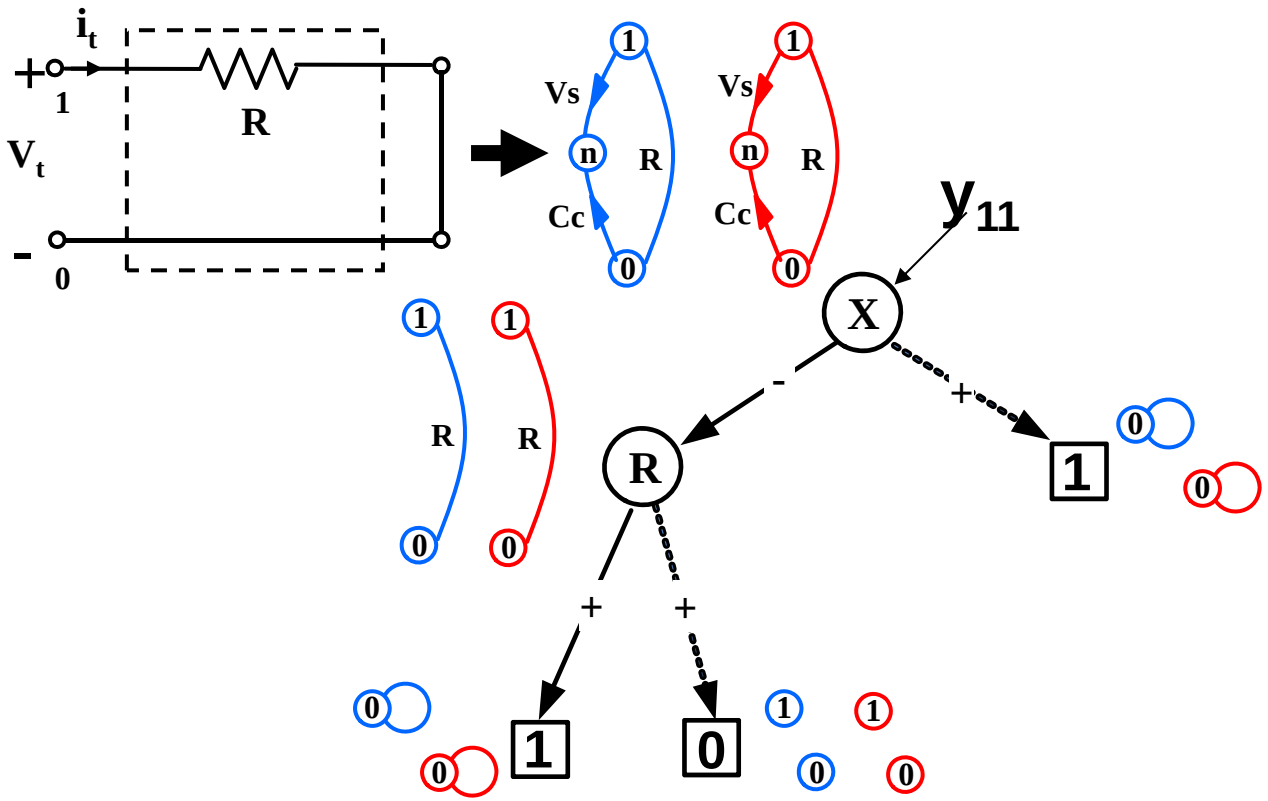

**A multi-root GRDD containing the 4 y-parameters**



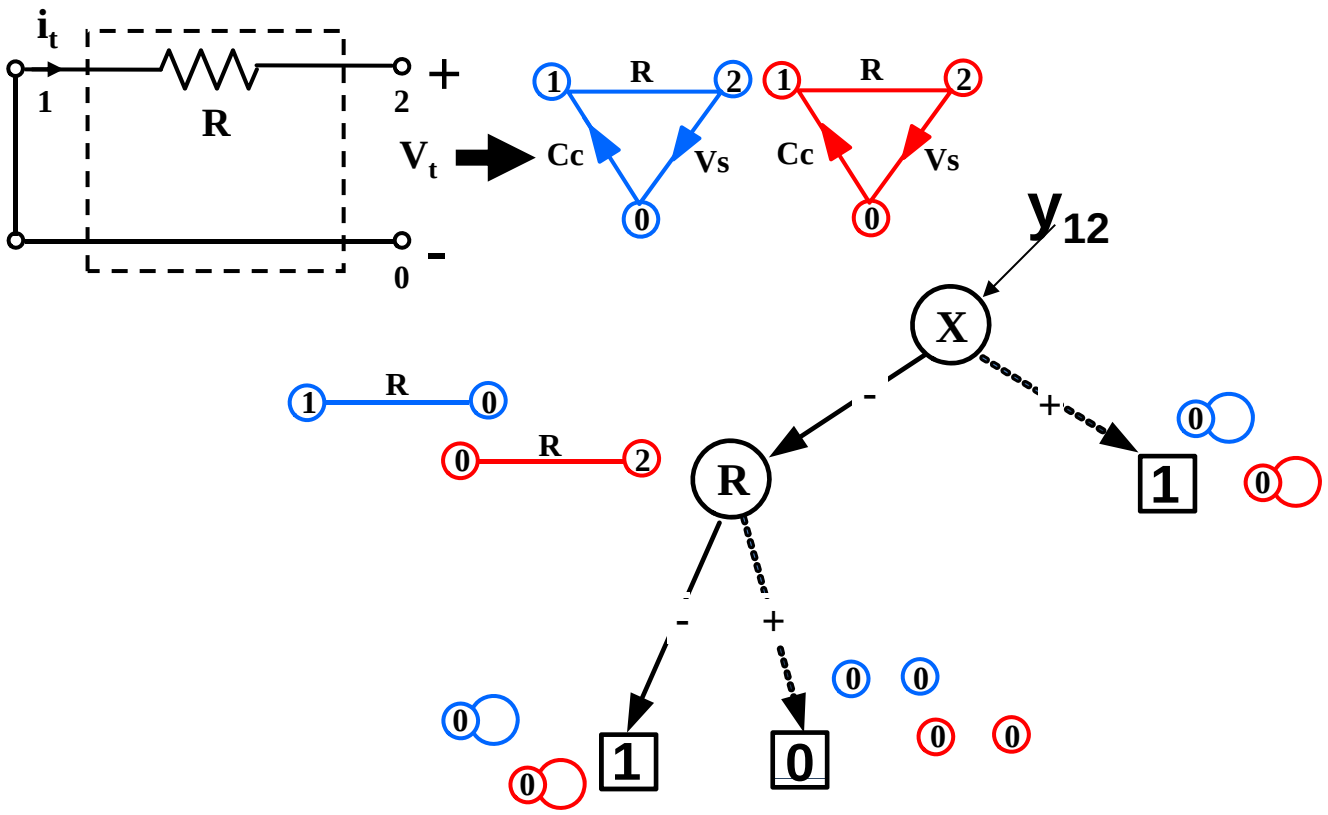

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} 1/R & -1/R \\ -1/R & 1/R \end{bmatrix}$$

**GPDD**

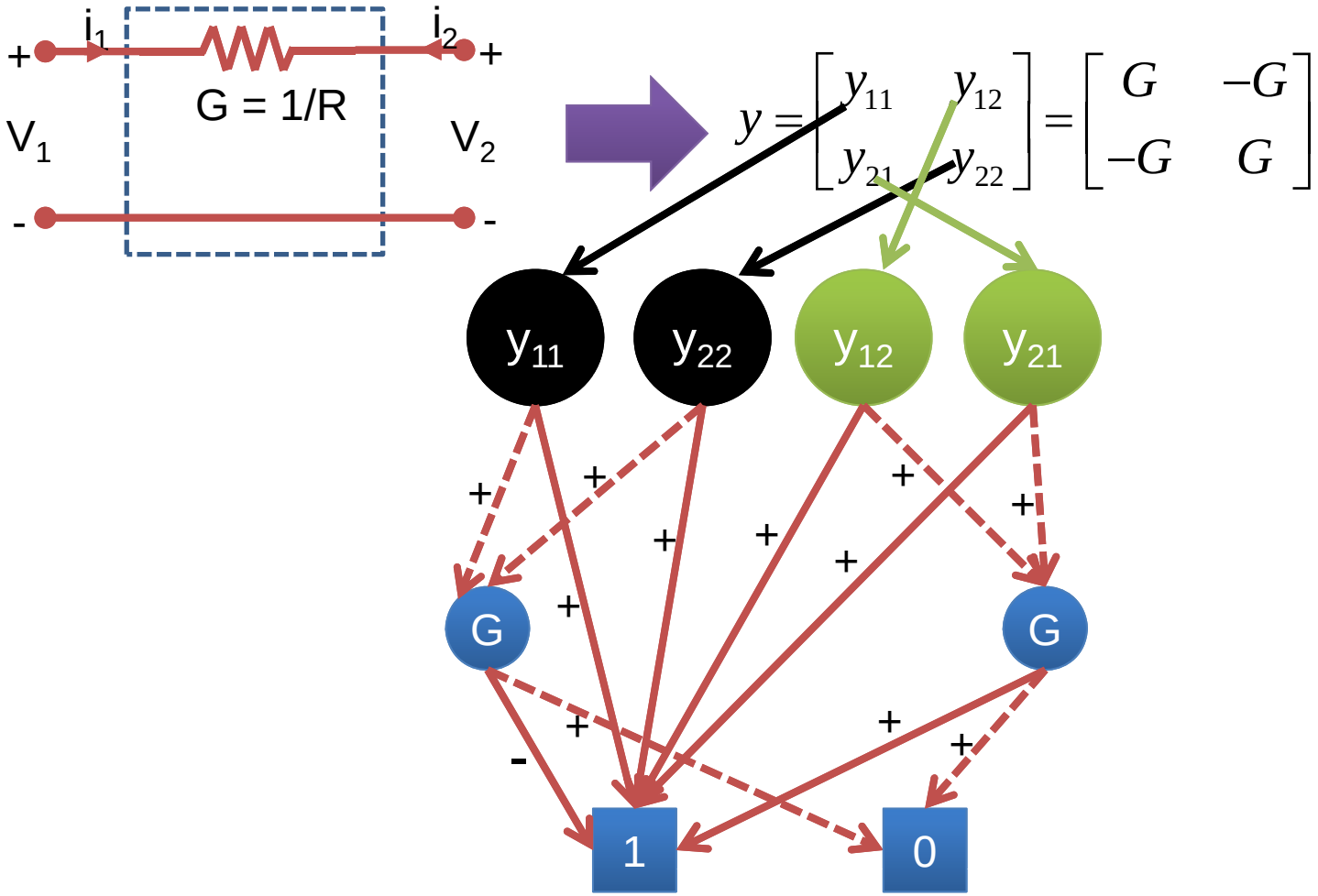
# Symbolic R Stamp ($y_{11}$)



# Symbolic R Stamp ($y_{12}$)

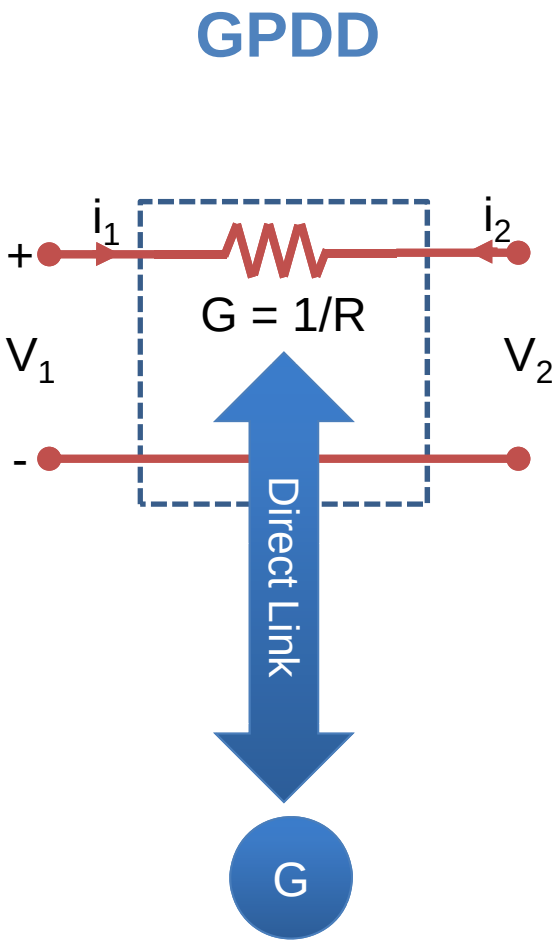


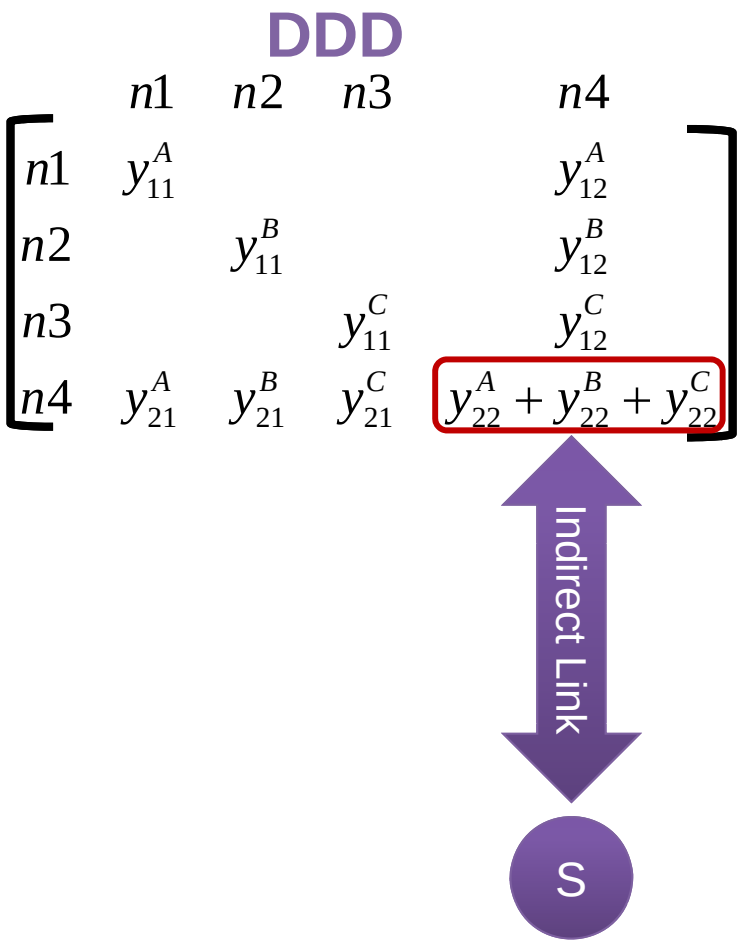
# Symbolic Stamp Computation



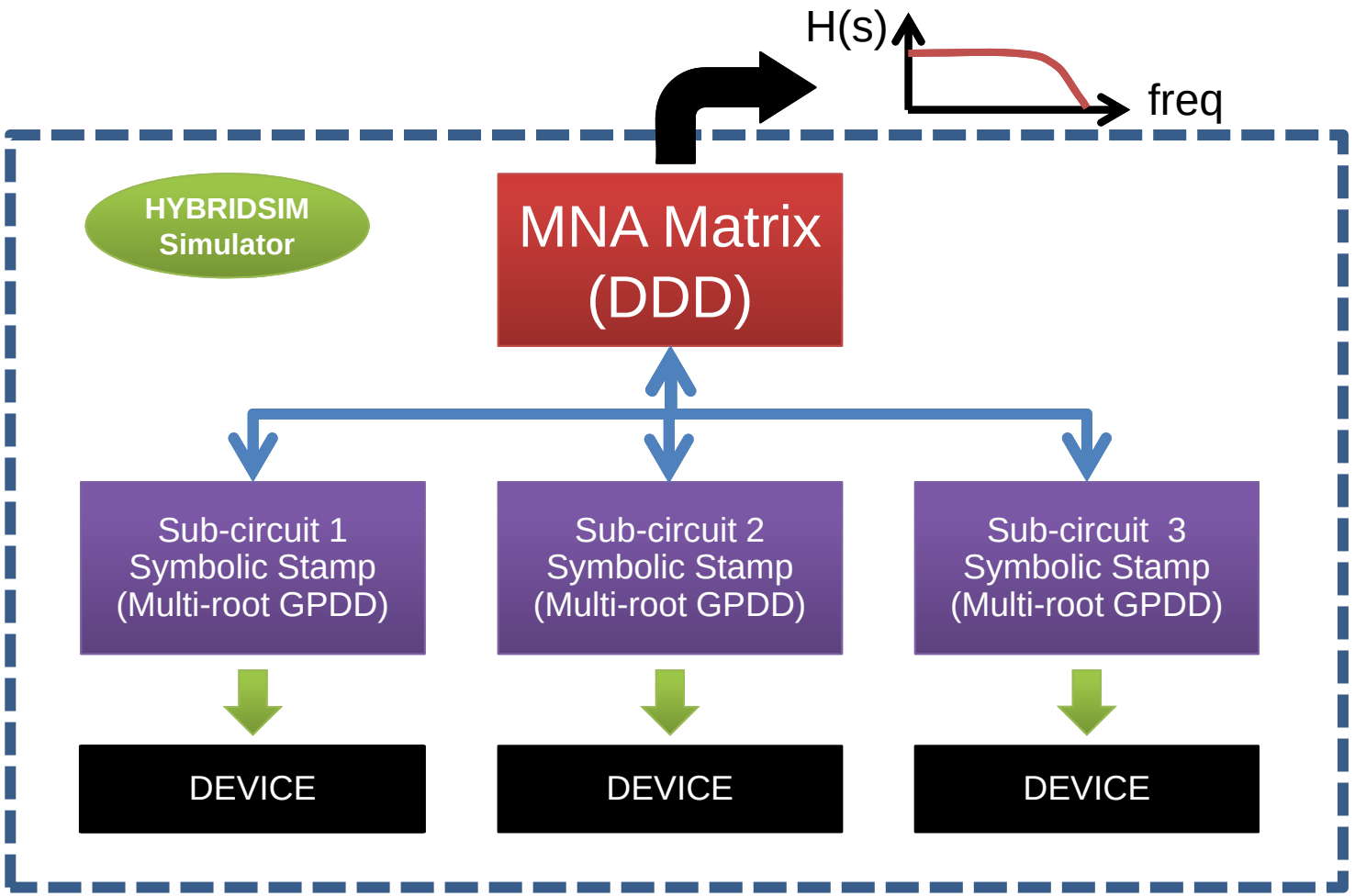

Four-root GPDD for R symbolic stamp

# Why GPDD for symbolic stamp



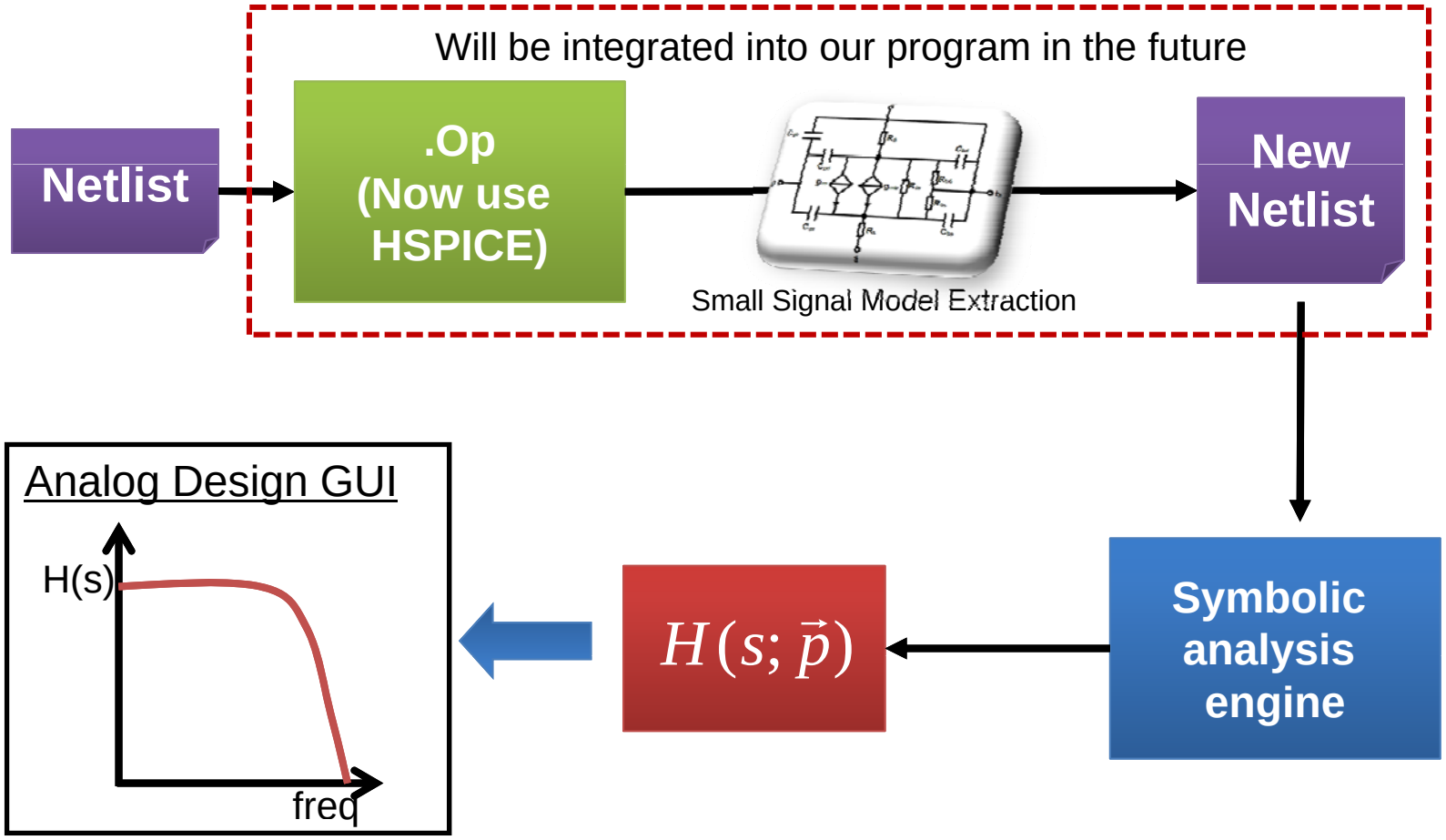



# Hierarchical Structure



# Experimental Results

# Implementation Flow

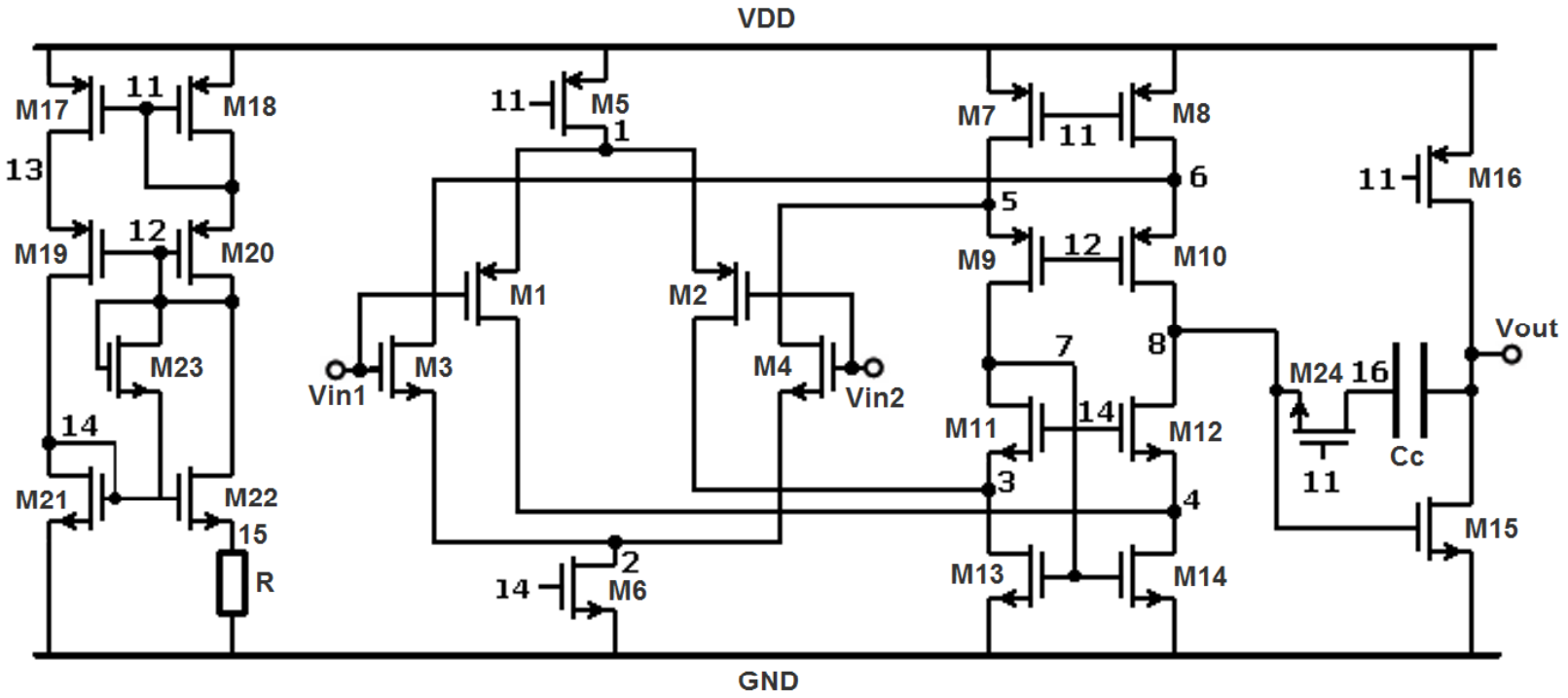


# Platform Environment

- Programming Language and tools:
  - C++
- Test cases are running on an AMD Athlon64 2.20GHz processor with 2GB memory
- HSPICE 2007 is used for DC operating point analysis

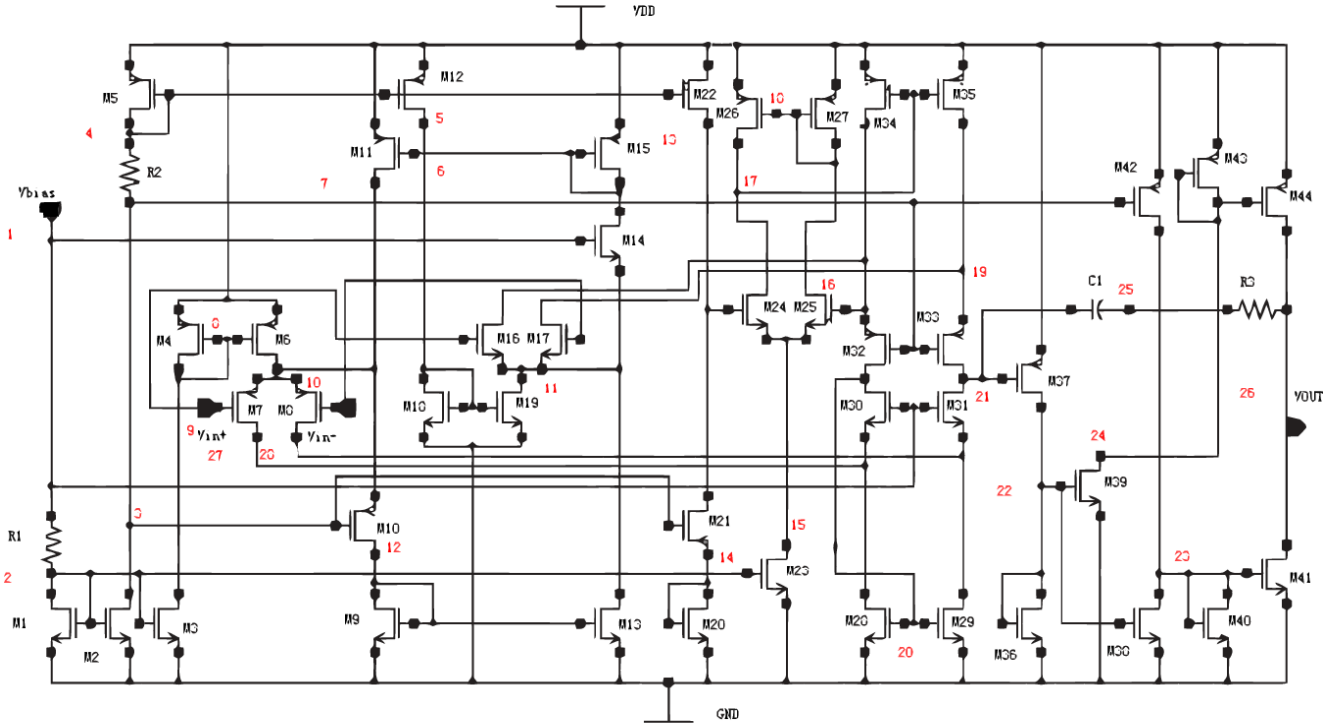
# Benchmark 1

- A rail-to-rail Miller MOSFET amplifier containing 24 transistors



# Benchmark 2

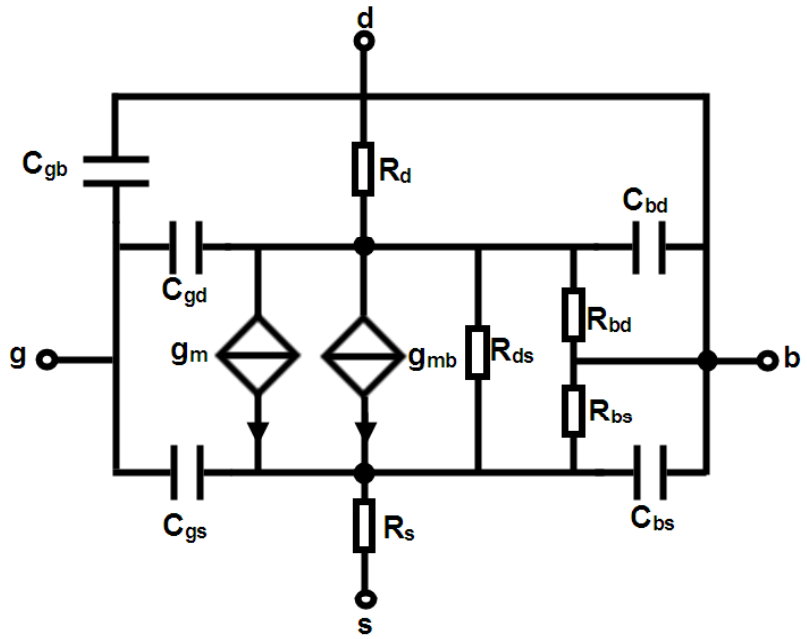
- A MOSFET operational amplifier containing 44 transistors[26]




[26] T. McConaghy and G. G. E. Gielen, “Globally reliable variation-aware sizing of analog integrated circuits via response surfaces and structural homotopy,” *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 28, no. 11, pp. 1627–1640, Nov. 2009.

# MOSFET Small Signal Model

- All MOSFETs share one symbolic stamp of the model

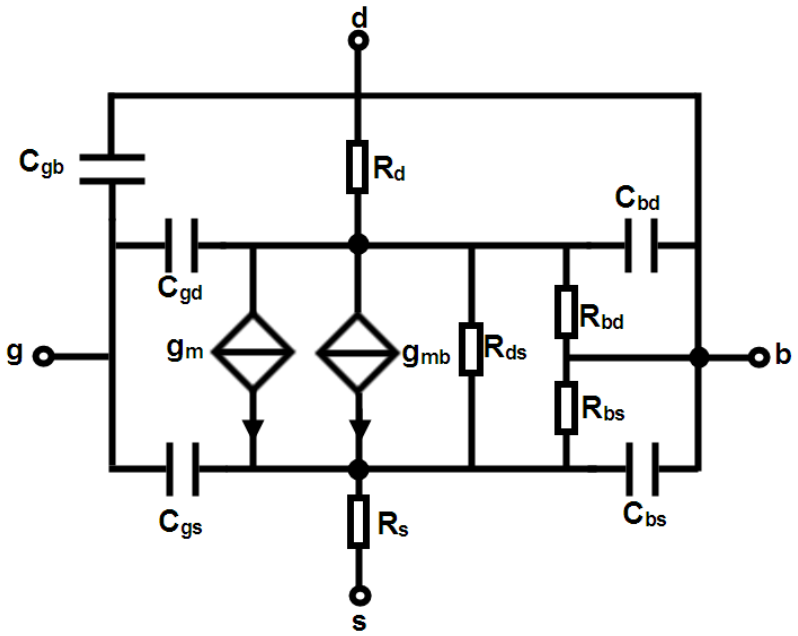



**■12 symbols**

**■481 vertices in the multi-root GRDD**

# Test Settings

- Partition Strategy
  - MOSFET as a sub-circuit
  - Maximize the sharing
- Small-signal Model
  - SPICE LEVEL 3[23]




[23] A. Vladimirescu and S. Liu, “The simulation of MOS integrated circuits using SPICE2,” EECS Department, University of California, Berkeley, Tech. Rep. UCB/ERL M80/7, 1980.

# Performance Summary

| Op-amp Circuit | #Device (T) | #Symb for GPDD | #Symb for DDD | MNA Matrix Size | \|GPDD\| (vertices) | \|DDD\| (vertices) | Time (sec.) | Memory (MB) |
|---|---|---|---|---|---|---|---|---|
| Case 1 | 24 | 12 | 104 | 18x18 | 481 | 70,129 | 1.81 | 70 |
| Case 2 | 44 | 12 | 140 | 28x28 | 481 | 45,716 | 1.50 | 91 |

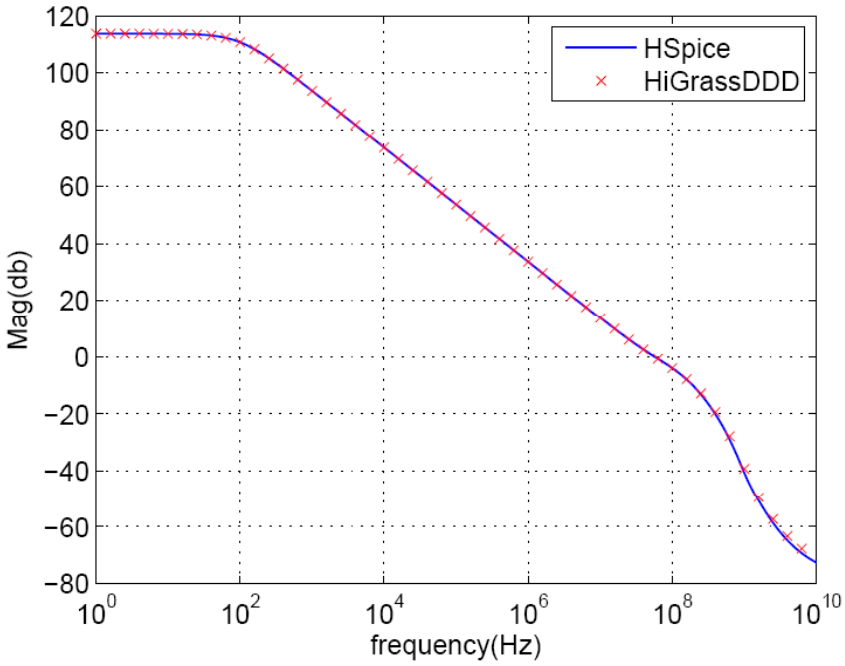
- Remarks
  - Both DDD-based (newly implemented[25]) and GPDD-based non-hierarchical simulator[16] cannot handle these two circuits.

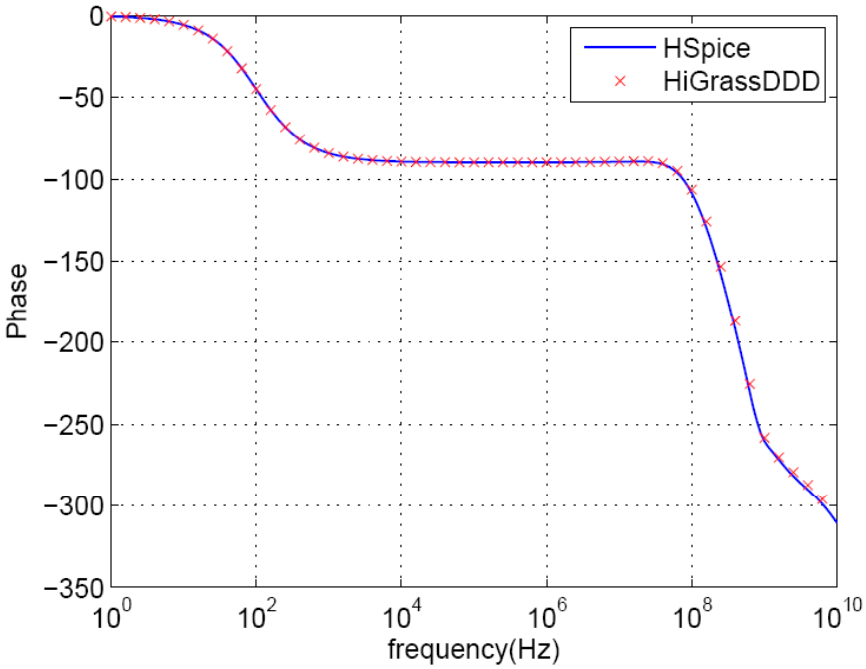

[16] G. Shi, W. Chen, and C.-J. R. Shi, “A graph reduction approach to symbolic circuit analysis,” in *Proc. Asia South-Pacific Design Automation Conference (ASPDAC)*, Yokohama, Japan, Jan. 2007, pp. 197–202.

[25] G. Shi, “A simple implementation of determinant decision diagram,” in *Proc. International Conf. on Computer-Aided Design (ICCAD)*, San Jose, CA, USA, Nov. 2010.

# Frequency Response

- **Benchmark 1 (24-trans rail to rail MOS amplifier)**



# Conclusion

- Proposed a “symbolic stamp” approach to hierarchical analysis
- Investigated an efficient implementation
- Improved the capacity for “exact” analysis
- More applications for design optimization in the future

# Thanks

Q & A