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Hierarchical Graph Reduction Approach to Symbolic Circuit Analysis with Data Sharing and Cancellation-Free Properties

Yang Song and Guoyong Shi
School of Microelectronics
Shanghai Jiao Tong University
Shanghai, China

Content

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- Principle of Symbolic Circuit Analysis
- BDD-based Symbolic Stamp Construction
- New Graph-based Hierarchical Method
  - Algorithm
  - Implementation
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- Summary

Symbolic Methods

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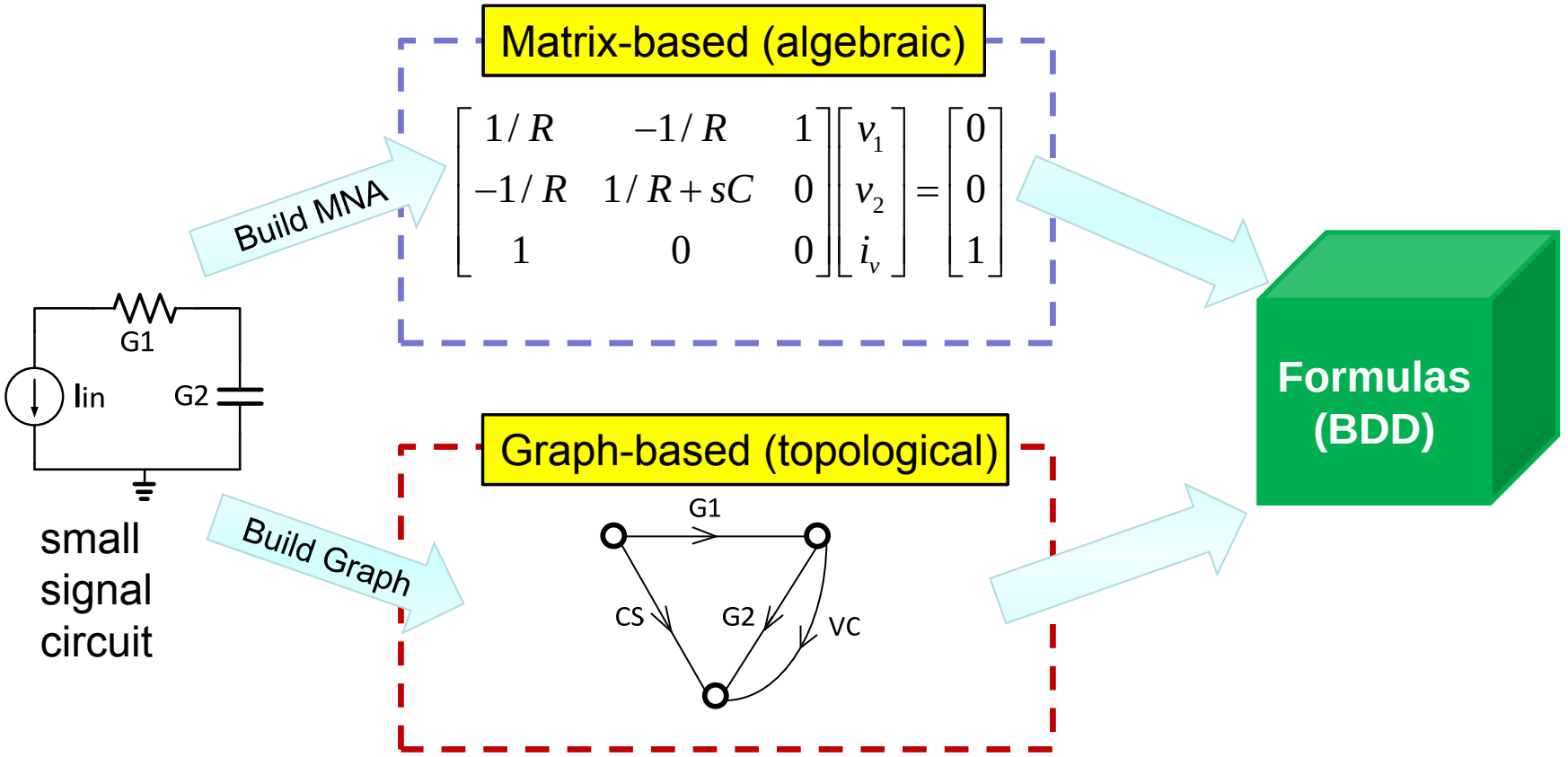
- From circuit to analytical formulas



BDD-based Methods

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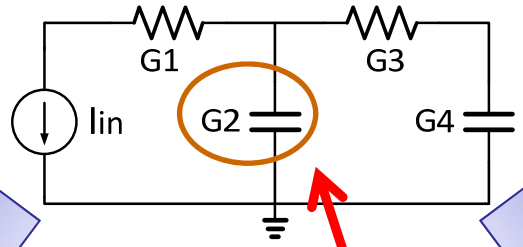
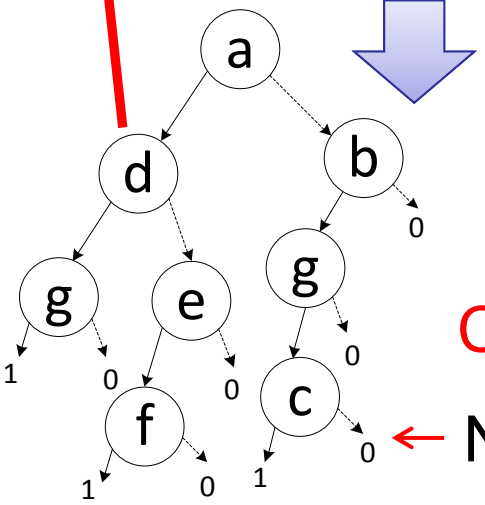
Determinant Decision Diagram (DDD)



Graph-pair Decision Diagram (GPDD)

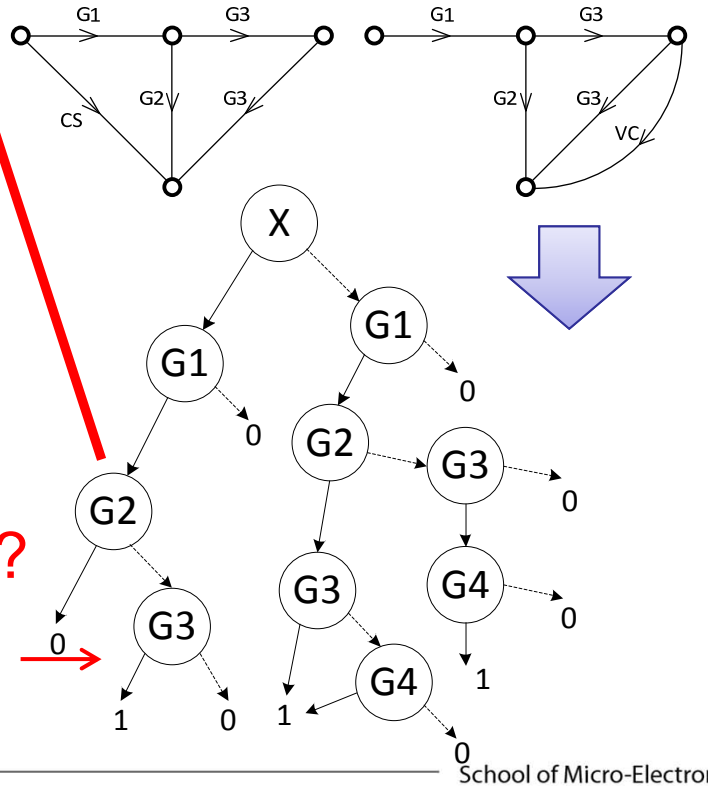
$$\begin{bmatrix} G_1 & -G_1 & 0 \\ -G_1 & G_1+G_2+G_3 & -G_3 \\ 0 & -G_3 & G_3+G_4 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} I_{in} \\ 0 \\ 0 \end{bmatrix}$$



Cancellation-free?

← No

Yes →



Motivation for Hierarchical Analysis

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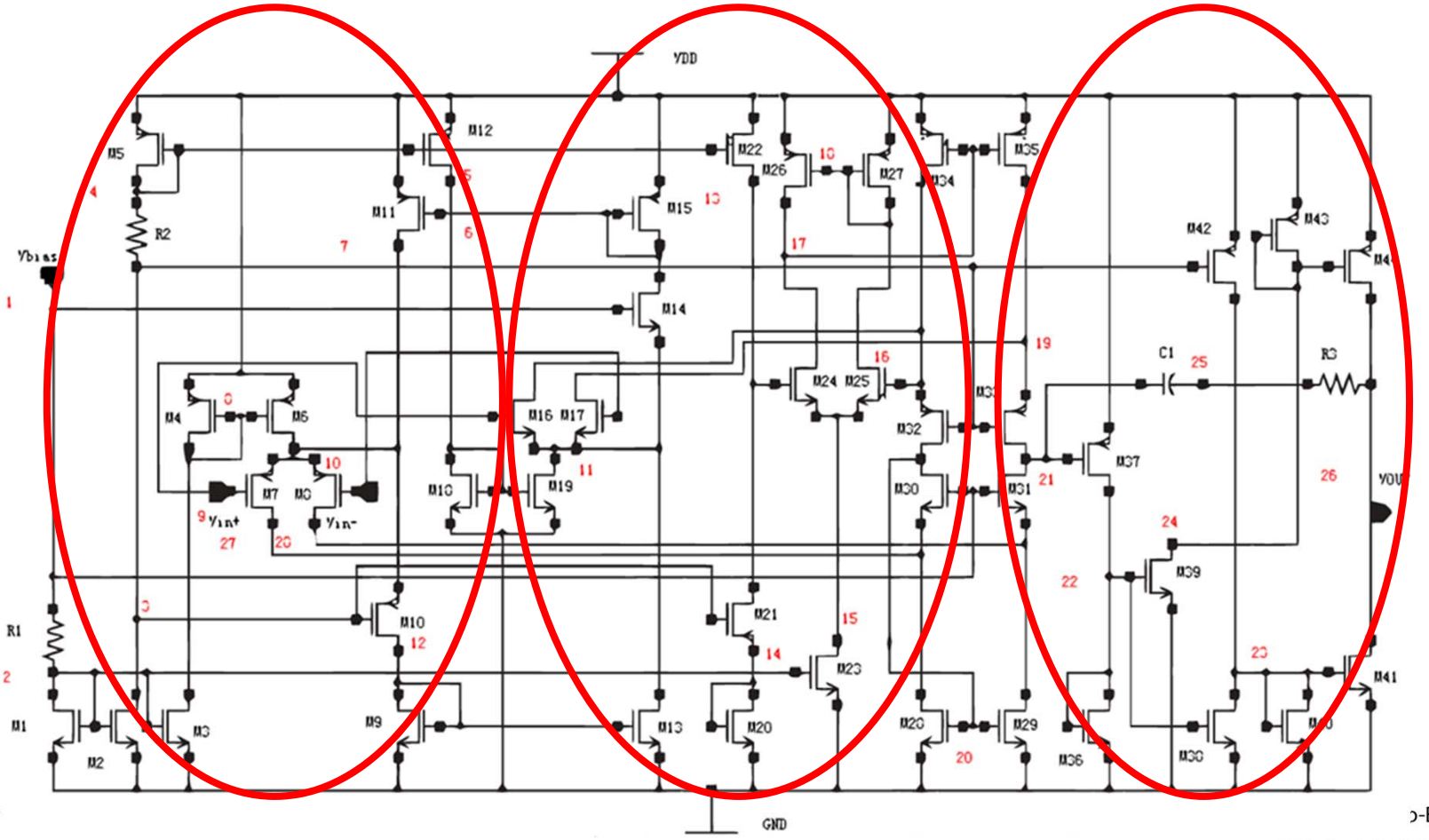
- When a circuit block is too large for flat symbolic analysis, we have to partition it and do hierarchical analysis.



Symbolic Stamp Construction

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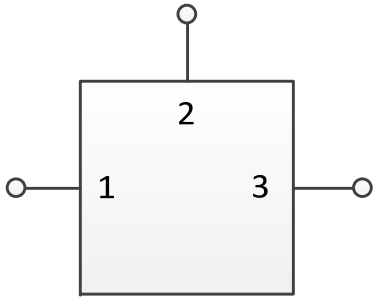
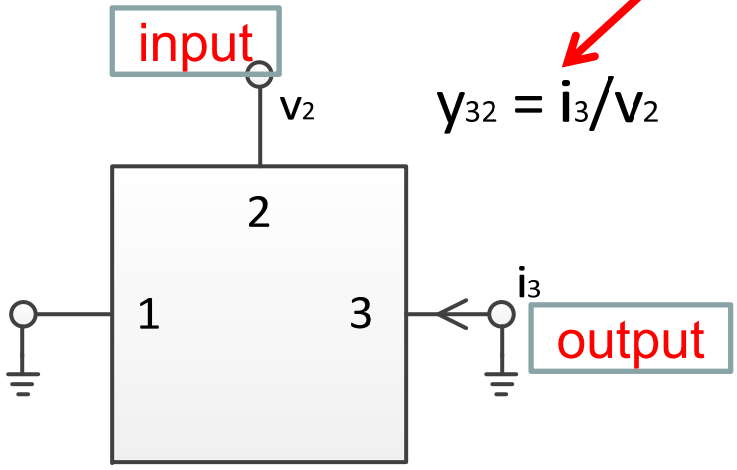
A 3-port circuit



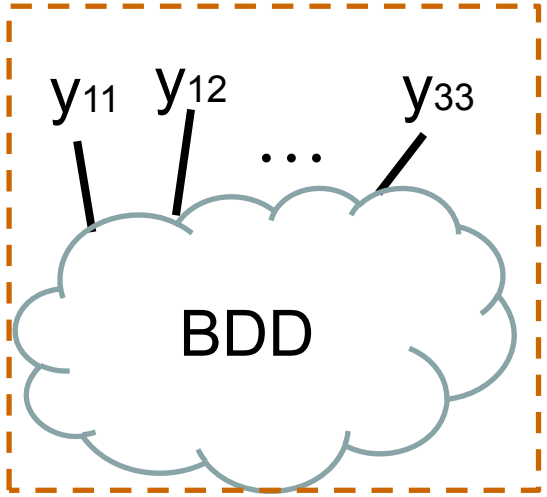
$$\begin{pmatrix} i_1 \\ i_2 \\ i_3 \end{pmatrix} = \begin{pmatrix} y_{11} & y_{12} & y_{13} \\ y_{21} & y_{22} & y_{23} \\ y_{31} & y_{32} & y_{33} \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \\ v_3 \end{pmatrix}$$

Trans-admittance Matrix / Y Matrix

$y_{32} = i_3/v_2$

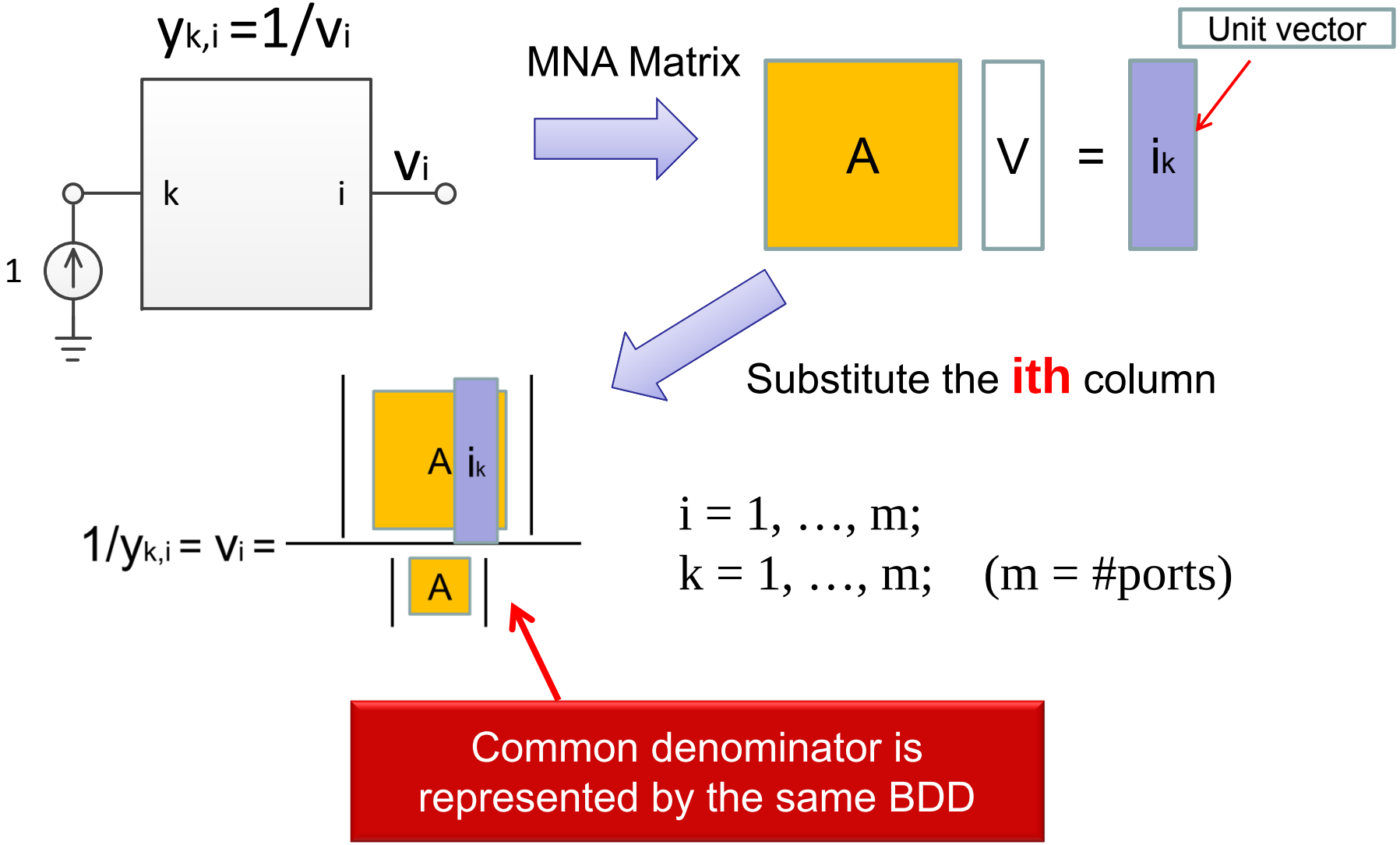


Symbolic Stamp



Multi-root DDD/GPDD

Symbolic Stamp by DDD



Symbolic Stamp by GPDD

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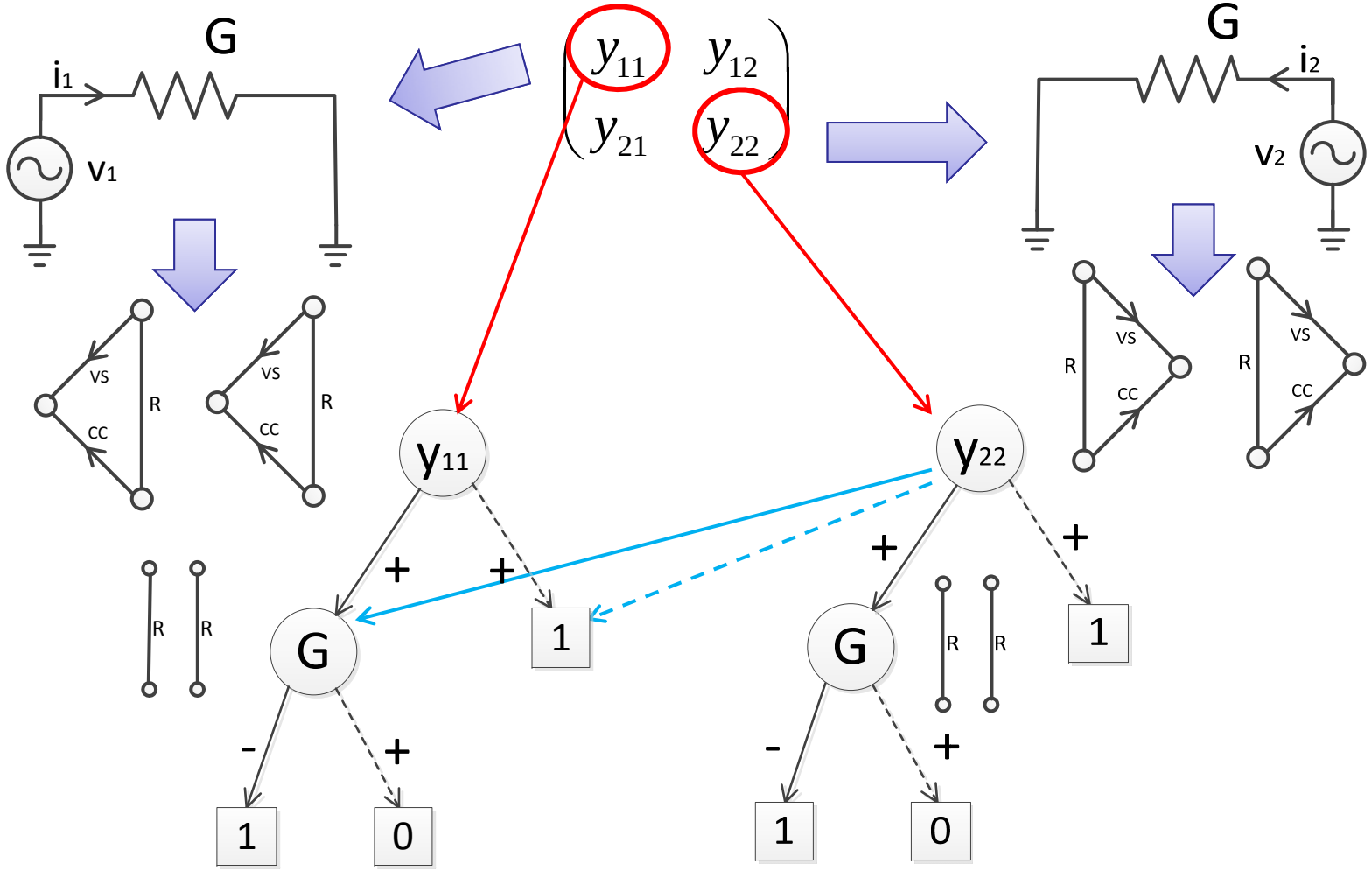

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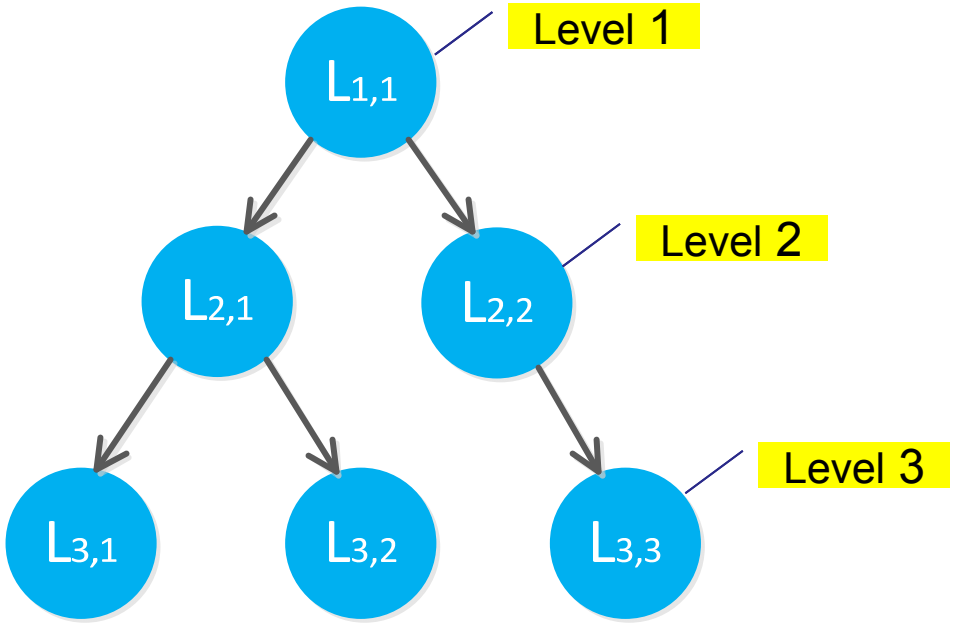
Hierarchical Analysis

- Break a large circuit into a nested hierarchy.
- Each module is described by a symbolic stamp.
- Assemble the symbolic stamps in analysis.



Each $L_{m,n}$ is a symbolic stamp.

Hierarchical Constructions

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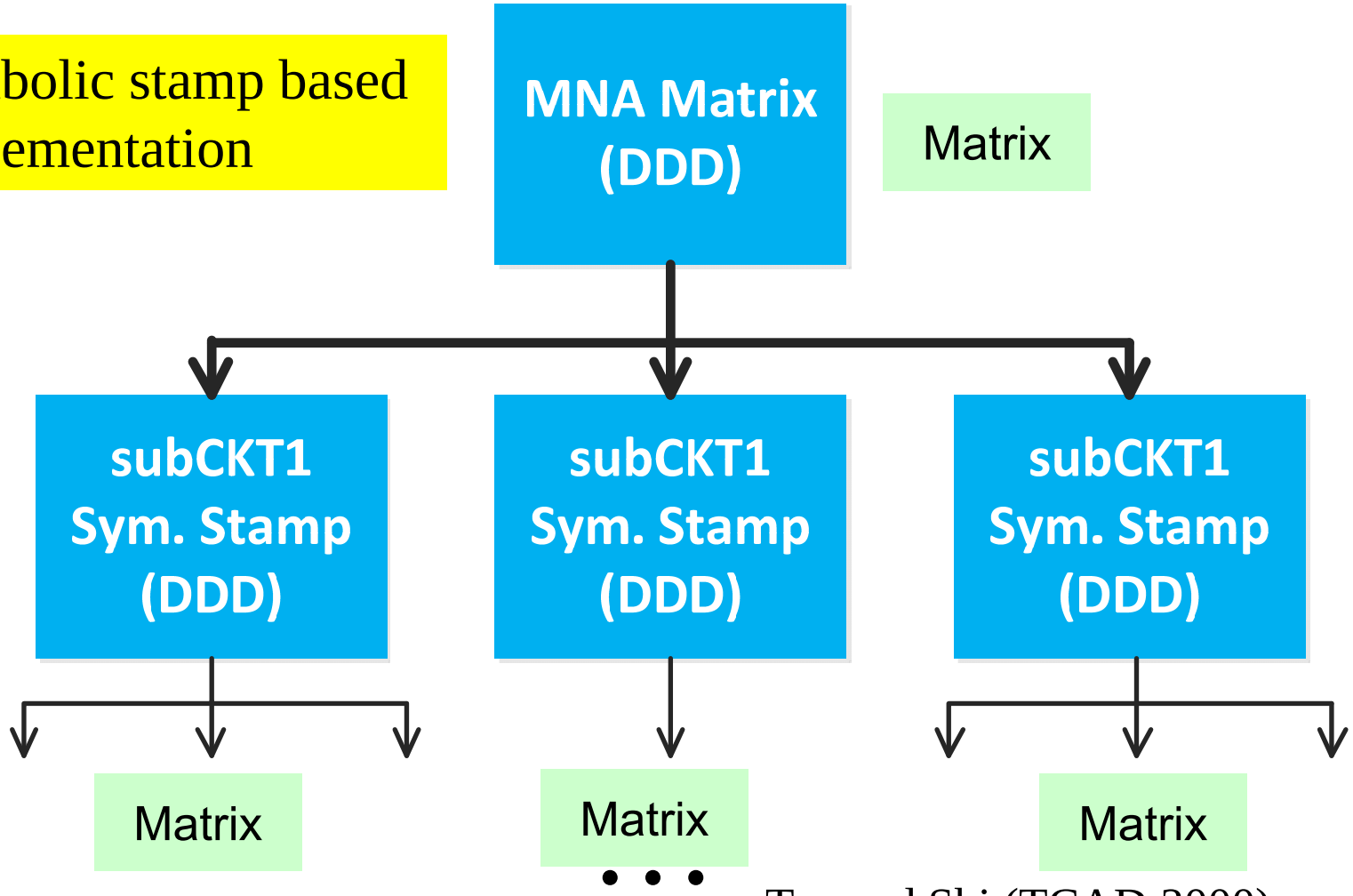
- Many ways of assembling symbolic stamps
- Typically we consider three methods:
  - Method 1: by hierarchical DDD (Tan-Shi TCAD 2000)
  - Method 2: by GPDD + DDD (Xu et al. ASPDAC 2011)
  - Method 3: **by hierarchical GPDD (this work)**

We mainly compare **Methods 1 and 3** in this work.

Method 1: Hierarchical DDD

Symbolic stamp based implementation



Tan and Shi (TCAD 2000)

Method 2: GPDD+DDD

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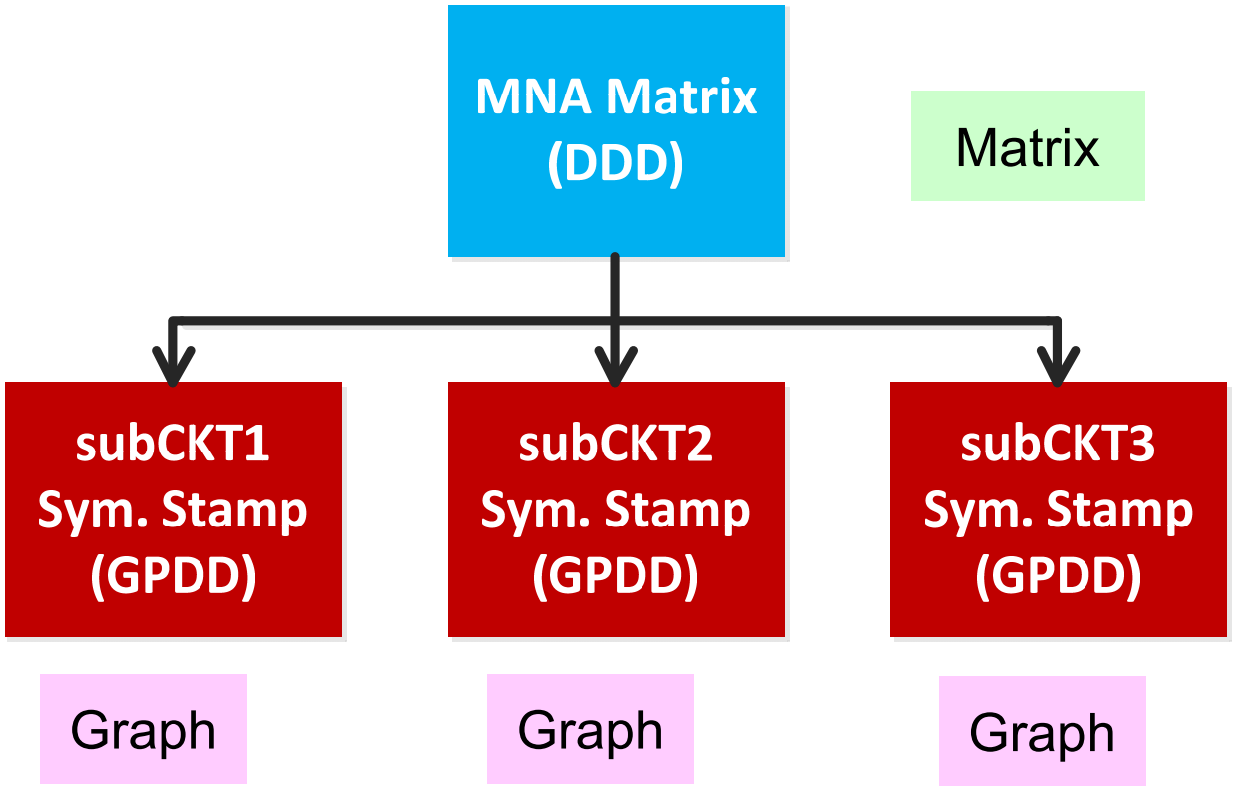
- Limitation: only two-layers



Xu, Shi, and Li (ASPDAC 2011)

Method 3: Hierarchical GPDD

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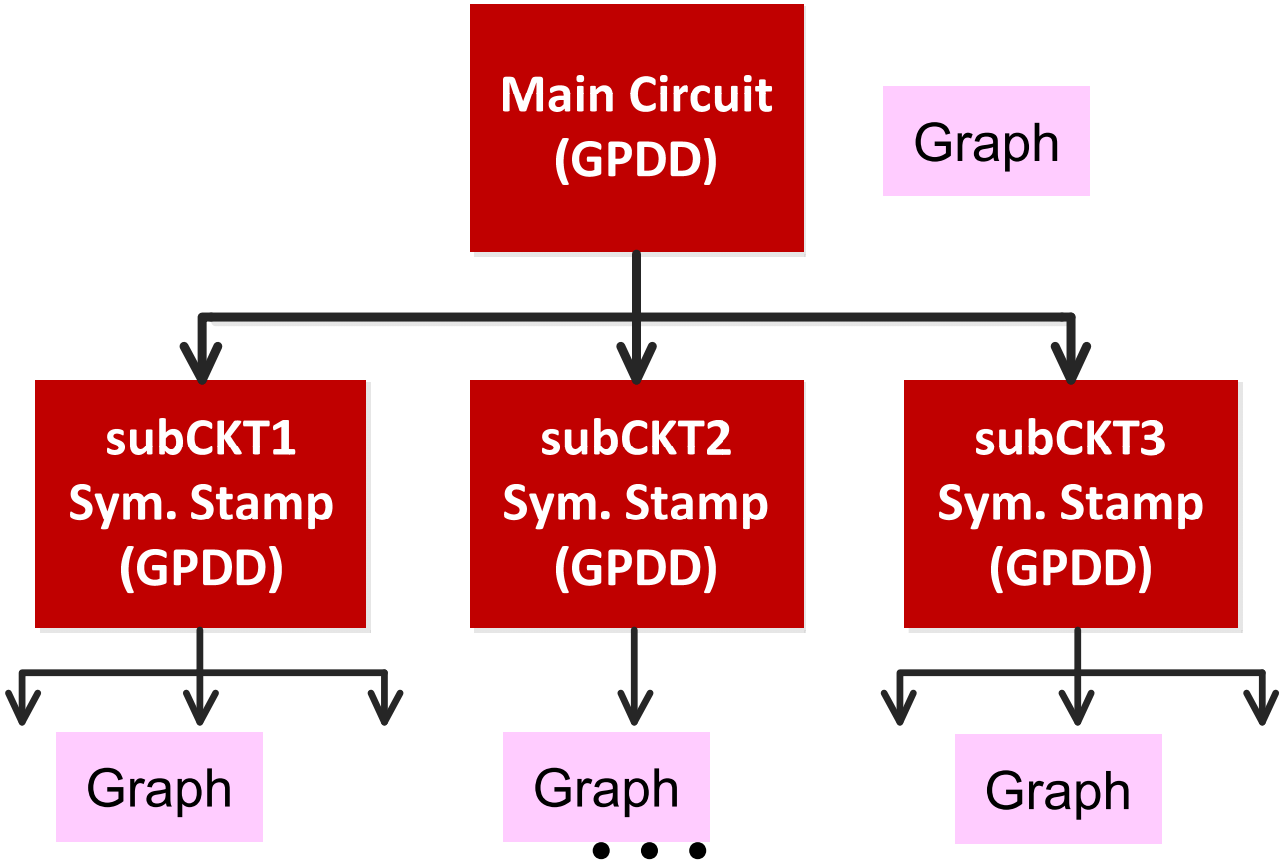
- **Contribution of this work**
- Purely graphical (based on circuit topology)



Key Technique

- A graphical treatment of m x m stamp (m > 1).

$$\begin{pmatrix} i_1 \\ i_2 \\ i_3 \end{pmatrix} = \begin{pmatrix} y_{11} & y_{12} & y_{13} \\ y_{21} & y_{22} & y_{23} \\ y_{31} & y_{32} & y_{33} \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \\ v_3 \end{pmatrix}$$

3x3 VCCS

1x1 VCCS

$$i_k = y_{k,m} v_m$$

A **3-port multi-dimensional VCCS** is treated as **nine** regular (1x1) VCCS's, among them 3 are admittances.

Each regular VCCS can be treated **by graph-pair reduction rules**. (Shi et al, ASPDAC 2006)

Experimental Results

- Implemented in C++
- Machine:
  - Intel Core2 Duo 1.80GHz processor
  - 2GB memory
- **Tested on three large operational amplifiers**
  - **Unsolvable by flat symbolic analysis**
  - **Compare two hierarchical methods**

μA725 – Partition 1

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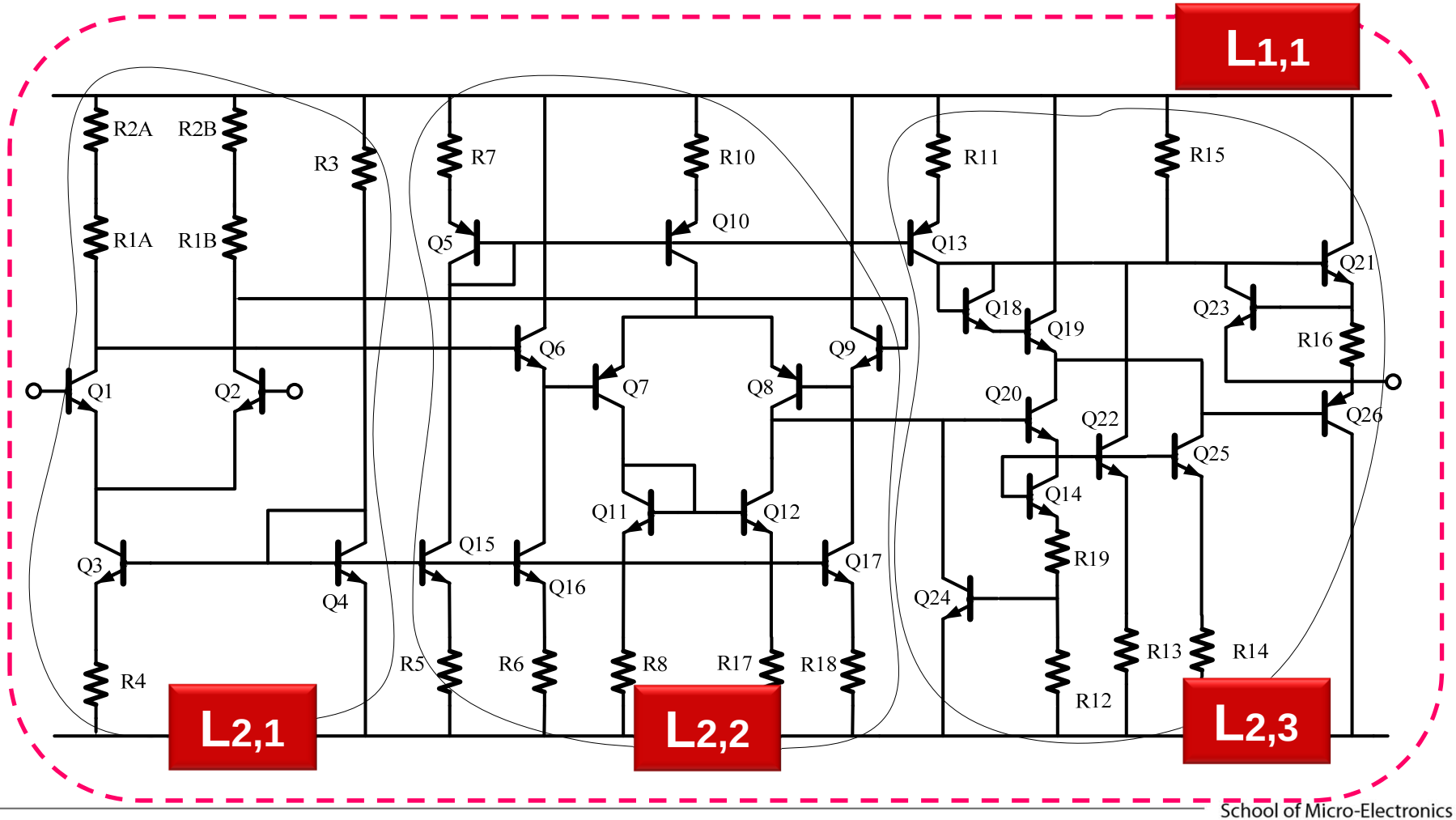
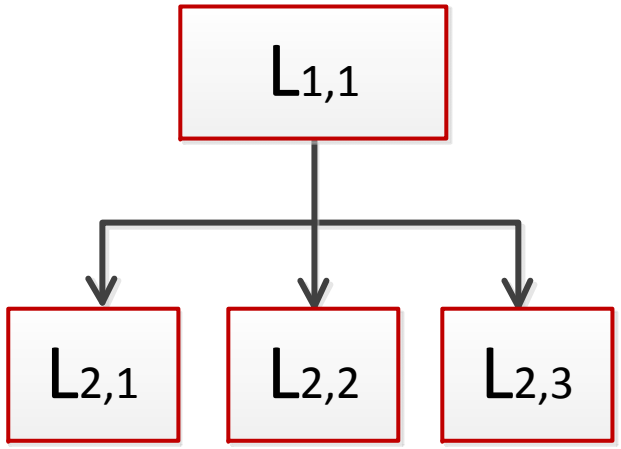
- Benchmark 1: μA725 opamp, containing 26 BJT transistors



Performance



Circuit Partition

Module	|GPDD|	GPDD Constr. Time (sec)
L1,1	773	0.016
L2,1	548	0.046
L2,2	135,785	**3.015**
L2,3	91,682	**2.067**
Total	**228,788**	**5.165**

μA725 – Partition 2

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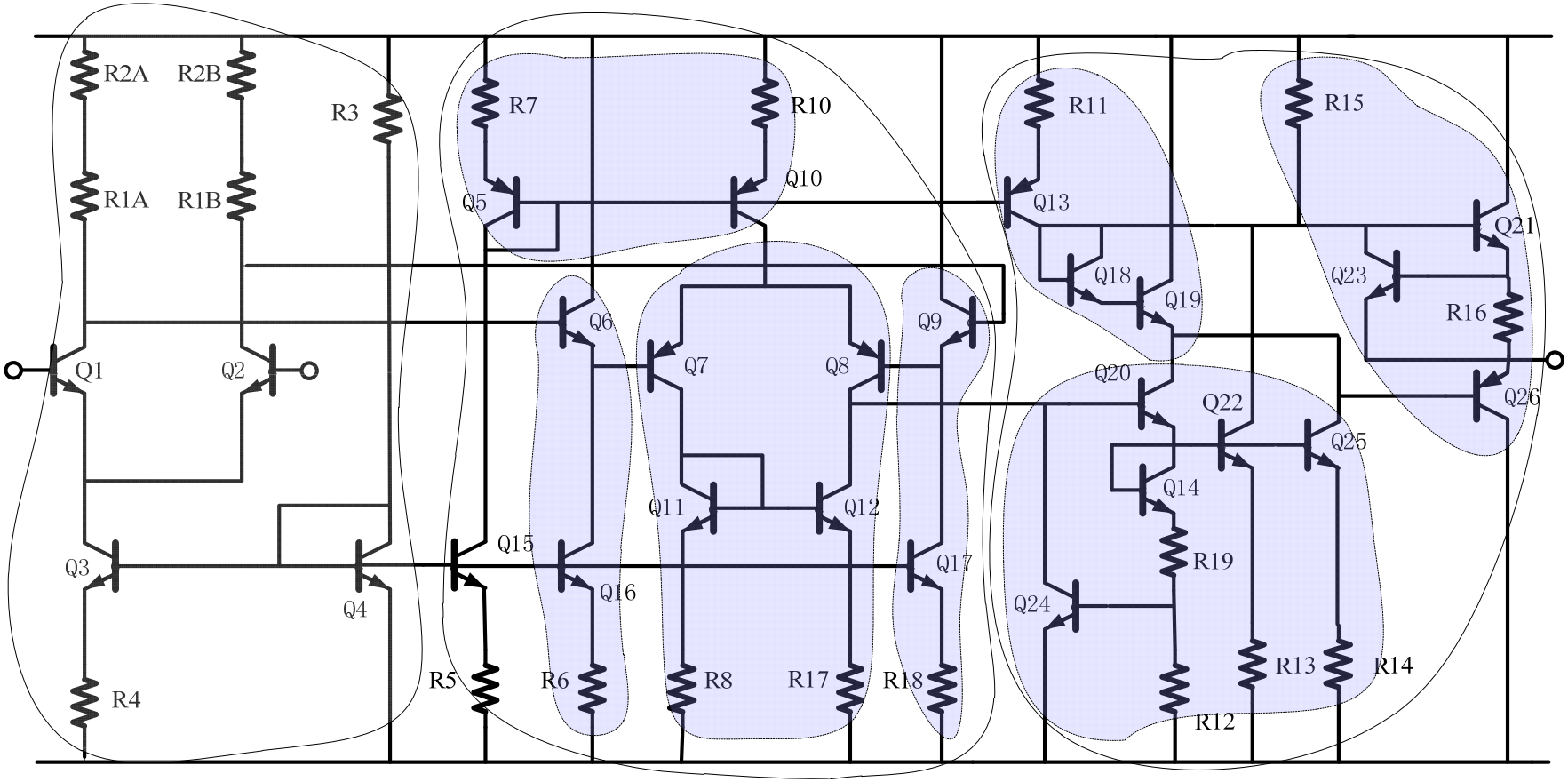

Performance

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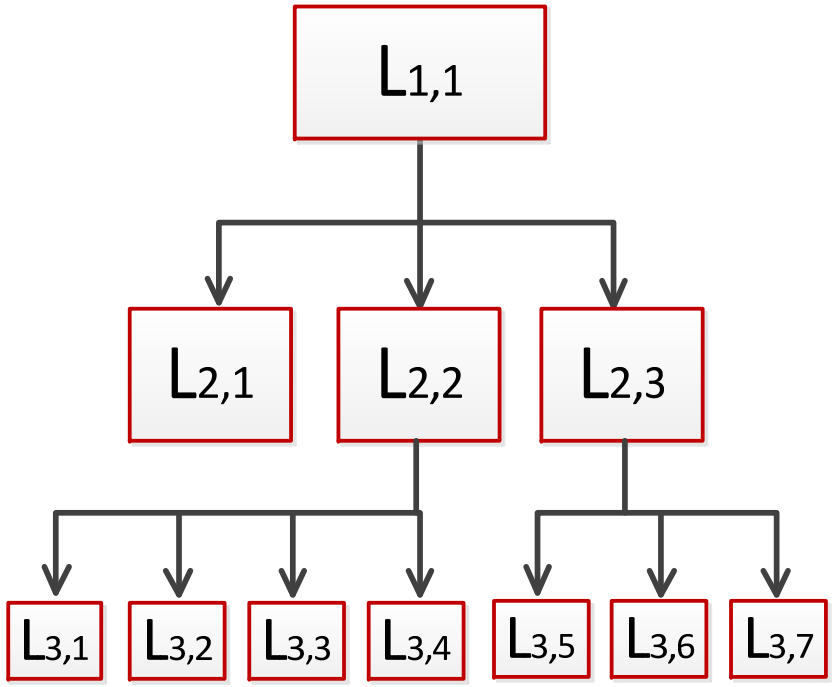
Circuit Partition



Module	|GPDD|	GPDD Time(s)
$L_{1,1}$	773	0.016
$L_{2,1}$	548	0.046
$L_{2,2}$	2,987	0.099
$L_{2,3}$	700	0.066
$L_{3,1}$	99	0.038
$L_{3,2}$	103	0.043
$L_{3,3}$	476	0.045
$L_{3,4}$	126	0.038
$L_{3,5}$	133	0.05
$L_{3,6}$	131	0.05
$L_{3,7}$	4,822	0.13
Total	**10,898**	**0.67**

Benchmark 2

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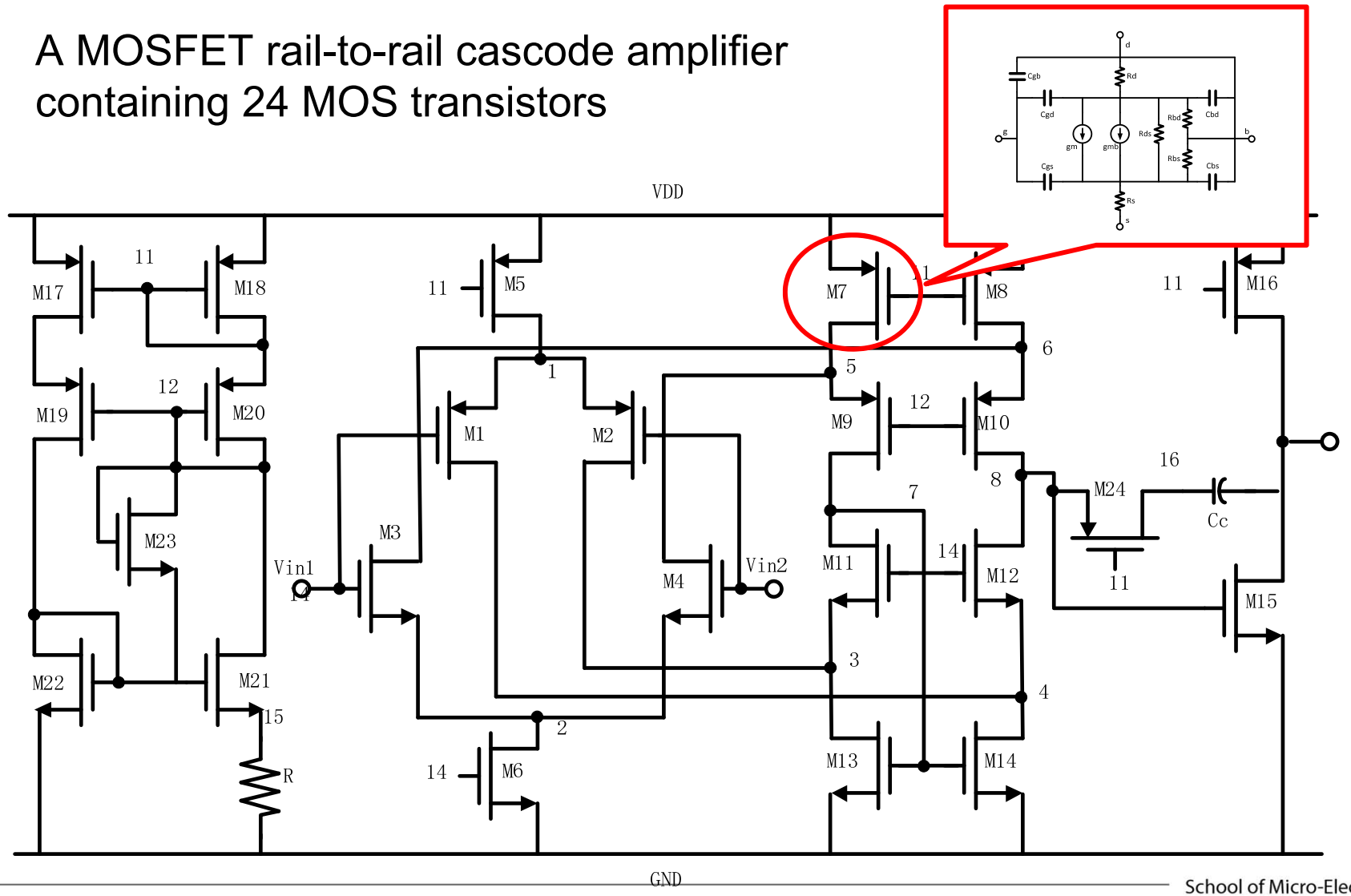
- A MOSFET rail-to-rail cascode amplifier containing 24 MOS transistors



Benchmark 3

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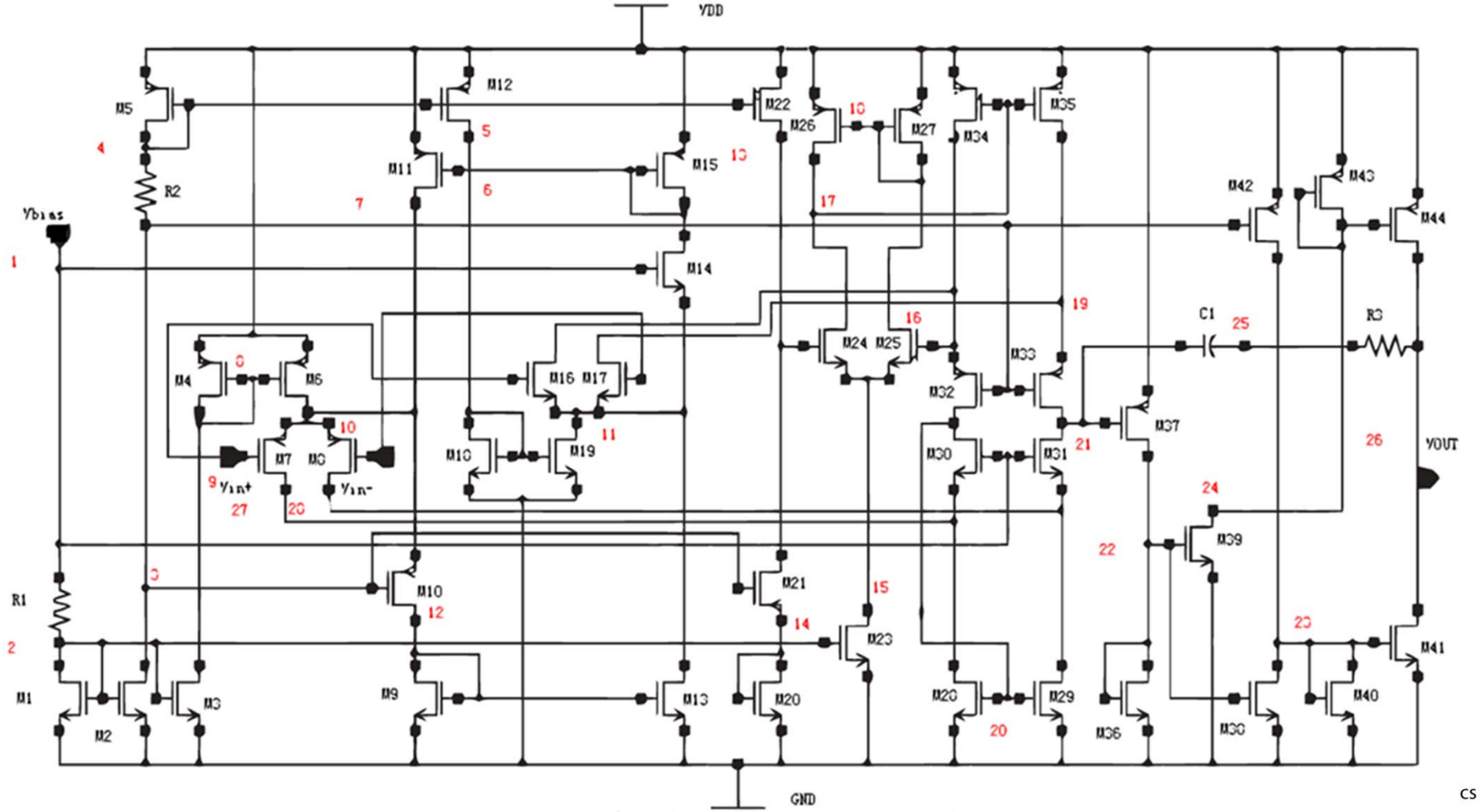
- A MOSFET amplifier with 44 MOS transistors



Hierarchical Partitions

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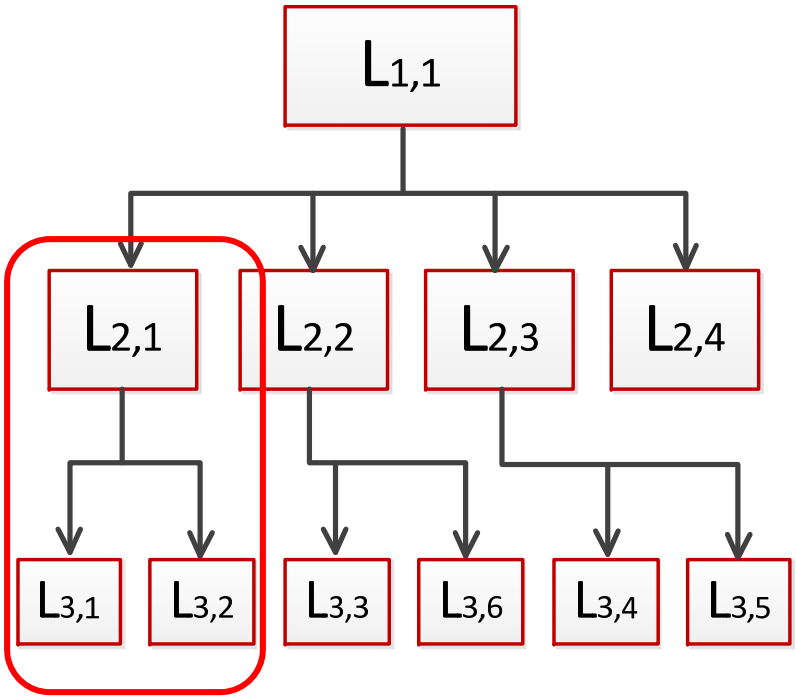
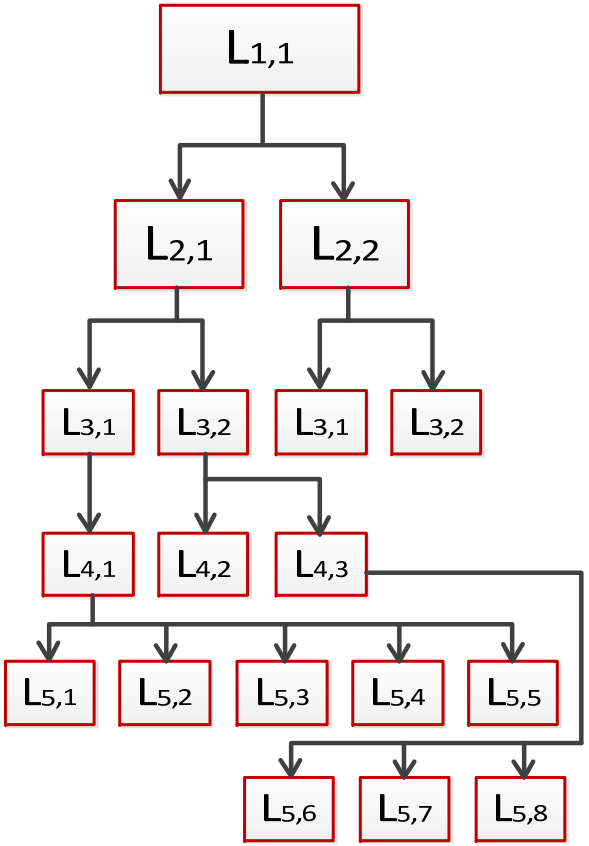
Benchmark 2



nested

Benchmark 3



Performance

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Comparison of construction time between methods 1 and 3 (method 2 does not apply.)

		Method 3		Method 1	
Circuit	#Levels	|GPDD|	GPDD Time(s)	|DDD|	DDD Time(s)
Benchmark 2	3	**17,488**	**0.793**	11,506	2.042
Benchmark 3	5	**197,274**	**6.771**	62,794	10.359

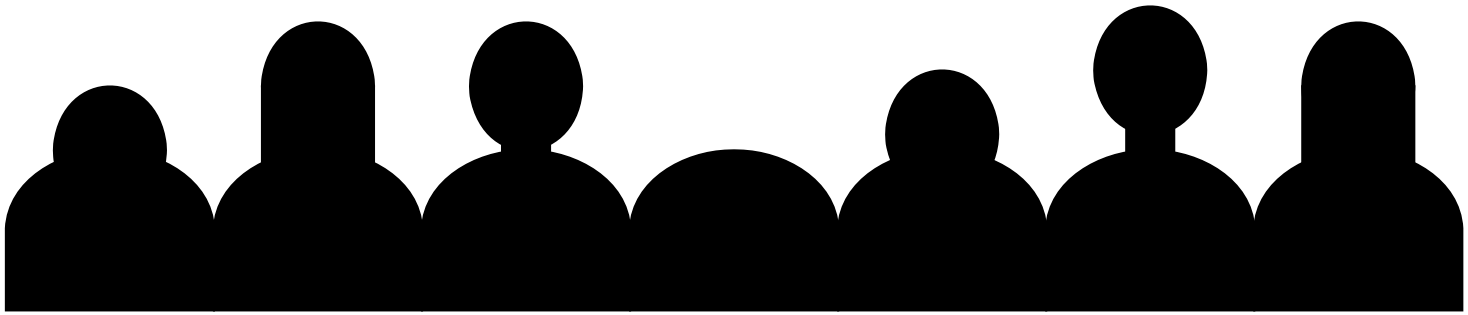
Comments

- Both hierarchical DDD and GPDD can solve large op-amp circuits.
- But the runtime performance of DDD or GPDD depends on the "symbol ordering" and the implementation details (e.g. hashing).
- **Other differences remain to be explored in design applications.**

Summary

- Proposed a new hierarchical symbolic method by graph reduction

- Compared two hierarchical methods (DDD/algebraic and GPDD/graphical)
  - Based on “symbolic stamp” implementations

Thanks

Q & A