

Statistical Full-Chip Dynamic Power Estimation Considering Spatial Correlations *

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ABSTRACT

Estimating the dynamic powers is crucial for power and energy efficient chip designs. With increasing variability from manufacture processes, dynamic powers can manifest significant variations due to uncertainties in device geometry and delay variations. In this paper, we propose a new statistical dynamic power estimation method considering the spatial correlation in process variation. We first show that channel length variation have significant impacts on the dynamic power of a gate. To consider the spatial correlation of channel length variation, we adopt a newly proposed spatial correlation model where a new set of uncorrelated variables are defined over virtual grids to represent the original physical random variables by least-square fitting. To compute the statistical dynamic power of a gate on the new set of variables, the new method applies the orthogonal polynomials based method. We use the segment-based statistical power method to consider impacts of the glitch variations on dynamic powers. The orthogonal polynomial of a statistical gate power is computed based on switching segment probabilities. The total full chip dynamic power expressions are then computed by summing up resulting orthogonal polynomials (their coefficients). Experimental results show that the proposed method has about 53X speedup over recently proposed statistical dynamic power analysis method and many orders of magnitudes over the Monte Carlo method.

1. INTRODUCTION

It is well accepted that the process-induced variability has huge impacts on the circuit performance in the sub-90nm VLSI technologies. The variational consideration of process has to be assessed in various VLSI design steps to ensure robust circuit design. Process variations consist of both inter-die ones, which affect all the devices on the same chip in the same way, and intra-die ones, which represent variations of parameters within the same chip. These include spatially correlated variations and purely independent or uncorrelated variations. Spatial correlation describes the phenomenon that devices close to each other are more likely to have similar characteristics than when they are far apart. It was shown that variations in the practical chips in nanometer range are spatially correlated [22]. Simple assumption of independence for involved random variables can lead to significant errors.

One great challenge from aggressive technology scaling is the increasing power consumption, which has become a major issue in VLSI design. And the variations in process pa-

rameters and timing delays result in variations in power consumption. Many statistical leakage power analysis methods have been proposed to handle both inter-die and intra-die process variation considering spatial variation [3, 11, 19, 23]. However, the problem is far from being solved for dynamic power estimation.

Dynamic power for a digital circuit in general is expressed as follows,

$$P_{dyn} = \frac{1}{2} f_{clk} V_{dd}^2 \sum_{j=1}^n C_j S_j \quad (1)$$

where n is the number of gates on chip, f_{clk} is clock frequency, V_{dd} is the supply voltage, C_j is the sum of load capacitance and equivalent short-circuit capacitance at node j , and S_j is the switching activity for gate j . This expression however, does not give explicit impacts of effective channel length (L_{eff}) and gate oxide thickness (T_{ox}) of the gate on the dynamic power. In the work of [10], L_{eff} and T_{ox} are proved to have the most impact on gate dynamic power consumption. Fig. 1 shows dynamic power variations due to

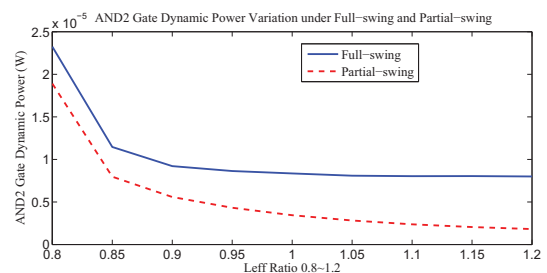


Figure 1: The dynamic power versus effective channel length for an AND2 gate in 45nm technology. (70ps active pulse as partial swing, 130ps active pulse as full swing)

different effective channel length for an AND2 gate in 45nm technology. It can be seen that channel length of a gate has a significant impact on its dynamic power.

In this paper, we propose to develop a more efficient statistical dynamic power estimation method considering channel length variations with spatial correlation and gate oxide thickness variations, which is not considered in the existing works. The new dynamic power analysis method explicitly considers the spatial correlations and glitch width variations on a chip. The new method follows the segment-based statistical power analysis method [7], where dynamic power is estimated based on the switching period instead of switching events to accommodate the glitch width variations. To consider the spatial correlation of channel length, we set up a set of uncorrelated variables over virtual grids to represent the original physical random variables via fitting. In this way, $O(n^2)$ time complexity for computing the variances can be reduced to linear time complexity (n is the number of gates in the circuit). The algorithm works for

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both strong and weak correlations. Furthermore, a look-up table (LUT) is created to cache statistical information for each type of gate to avoid running SPICE repeatedly. The proposed method has no restrictions on models of statistical distributions for dynamic powers. Experimental results show that the proposed method has 53X speedup over recently proposed method [7] and many orders of magnitudes over the Monte Carlo method.

2. PRIOR WORKS

2.1 Existing relevant works

Many works on dynamic power analysis have been proposed in the past. Monte Carlo based simulation was proposed in [2] where the circuit is simulated for a large number of input vectors to gain statistics for average power. Later, probabilistic methods for power estimation were proposed and widely used [6, 9, 13, 14, 21] because statistical estimates can be obtained without time-consuming exhaustive simulation. In [14], the concept of probability waveforms is proposed to estimate the mean and variance of the current drawn by each circuit node. In [13], the notion of transition density is introduced and they are propagated through combinational logic modules without regard to their structure. However, the author did not consider the inner signal correlation, thus the algorithm is only applicable to combinational circuits. Ghosh et al. [9] extended the transition density theory to consider sequential circuits via the symbolic simulation to calculate the correlations between internal lines due to reconvergence. However, the performance of this algorithm is restricted due to its memory space complexity. In [6, 21], the authors used the tagged probabilistic simulation (TPS) to model the set of all possible events at the output of each circuit node and is more efficient compared with [9] due to its effectiveness in computing the signal correlation. The work [9] is based on zero-delay model and the works [2, 13, 21] are based on real delay model. However, all of them assume fixed delay model, which is no longer true under process variation. At the same time, all the previous works only consider full-swing transition and partial-swing effects are not well accounted for.

Recently, several approaches have been proposed for fast statistical dynamic power estimation [1, 5, 7, 10, 12, 17]. Alexander et al. [1] proposed to consider the delay variations and glitches for estimation dynamic powers. With efficient simulation of input vectors, this algorithm has a linear time complexity. But the variation model is quite simple as only minimum and maximum bounds for delay were obtained, and partial swings are not considered. Pilli et al. [17] presented another approach, which divides the clock cycle into a number of time slots and the transition density is computed for each slot, but only mean value of dynamic power can be estimated. In [12], the authors used supergate and timed Boolean functions to filter glitches and consider signal correlations due to re-convergent fanouts, but failed to consider the correlations including placement information. Chou et al. [5] used probabilistic delay model based on Monte Carlo simulation technique for dynamic power estimation, also lacks the considerations including placement information. Harish et al. [10] used hybrid power model based on Monte Carlo analysis, the method is only applied to a small two-stage 2-input NAND gate, however, for large circuits, Monte Carlo simulation can be really time consuming.

2.2 Segment-based power estimation method

Dinh et al. [7] recently proposed a method not based on the fixed delay gate model to consider the partial-swing effect as well as the effect of process variation.

To accurately estimate the dynamic power in the presence of process variation, the work in [7] introduces the *transition waveform* concept, which is similar to the probability

waveform [14] or tagged waveform [6] concepts except that variance of the transition time is introduced. Specifically, a transition wave consists of set of transition event, which is a triplet (p, t, δ_t) where p is the probability for the transition to occur, t is the mean time of the transition and δ_t is the standard deviation of the transition time. Fig. 2 shows an example of transition waveform for a node.

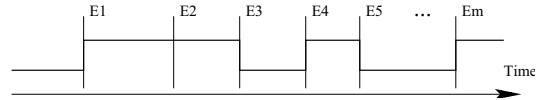


Figure 2: A transition waveform example $\{E_1, E_2, \dots, E_m\}$ for a node

The triplets are then propagated from the primary inputs to the primary outputs and they are computed for every node. In addition to propagating the switching probabilities like tradition methods, this method also propagates the variances along the signal paths, which is done in straight forward way based on the second order moment matching. The glitch filtering is also performed to ensure accuracy and reduce the number of switches during the propagation.

Unlike the traditional power estimation methods in [6, 14], which count the transition times (or their probabilities), i.e. edges in the transition waveform, to estimate the dynamic power, the work in [7] proposed to count the transition segments (duration), which are pairs of two transition events to take into account of the impacts of the different glitch widths on the dynamic power consumption. For n transition events in transition waveform, the number of segments is $C_n^2 = n(n-1)/2$, which increases the complexity of the computation compared to the edge-based method. Another implication is traditional power edge-based consumption formula (1) can't be used any more. As a result, a look-up table is built from the SPICE simulation results for different glitch widths. The total dynamic power for a gate is then the probability-weighted average dynamic power for all the switching segments, which is then summed up to compute the total chip dynamic power. However, this method does not consider spatial correlation, which can lead to significant errors and is the main issue to be addressed in this paper.

3. VARIATIONAL MODELS FOR PROCESS PARAMETERS

Following the existing approaches, we also assume that the process variations of L and T_{ox} follow multivariate normal distributions [20], and both of them include inter-die and intra-die components. Since T_{ox} is in vertical layout feature dimension, and is caused by chemical mechanical polishing processes, it only depends on local layout density and has no spatial correlation [16]. Therefore, we focus on the spatial correlation of L . In general, the number of process parameters that exhibit spatial correlation can be more than one, and it is understood that this is not a limitation of our approach.

The spatial correlation used in this paper is given by the following empirical exponential model [22].

$$\rho(d) = e^{-d^2/\eta^2}, \quad (2)$$

where d is the distance between two grid centers and η is called the *correlation length*. Large η means the spatial correlation is strong, vice versa. The spatial correlation can be captured by the spatial covariance matrix $\Omega_{n,n}$, where n is the number of gates on chip. The elements in $\Omega_{n,n}$ are modeled as (2), which are only related to d . Dealing with spatial correlation leads to quadratic computations as all the correlated variables are enumerated pairwise for accurate variance estimation.

Spatial correlation makes the statistical computation to be quadratic as every pair of gates has to be considered

to accurately estimate statistical information such as variance. To mitigate this problem, some approaches have been proposed in the past. One way is to partition the circuit into many grids where all correlated variables in a grid will be represented by one grid variable [3]. Another way is by means of the variable reduction technique (by principal component analysis) [19]. The limitation is that both methods achieve linear time complexity in terms of gates only in case of strong spatial correlation. In this paper, we use virtual grid based spatial correlation modeling technique. It works for both weak and strong correlations for achieving linear time complexity for statistical information computation (see more on Subsection 4.2).

In addition to the variations in L and T_{ox} , we also have the variations of glitch width due to the delay variations obtained during the propagation along signal paths. Specifically, for a switching segment defined by the two transitions (t_1, σ_{t_1}) and (t_2, σ_{t_2}) propagating through a gate or wire, glitch width is assumed to be of normal distribution with mean μ_w and standard deviation σ_w : $\mu_w = t_2 - t_1$, $\sigma_w = \sqrt{\sigma_{t_1}^2 + \sigma_{t_2}^2}$. In summary, in our variational model, we consider three variation sources: channel length L , oxide thickness T_{ox} , glitch width W_g .

4. THE NEW STATISTICAL DYNAMIC POWER ESTIMATION METHOD

4.1 Flow of the proposed analysis method

In this section, we present the new full-chip statistical dynamic power analysis method. The new approach follows the segment-based power estimation method [7]. The new algorithm propagates the triplet switching events from primary input to the output. Then it computes the statistical dynamic power at each node based on orthogonal polynomials and virtual grid-based variables for channel length to deal with spatial correlation. We first present the overall flow of the proposed method in Fig. 3, and then highlight the major computing steps later.

Algorithm: NEW FULL-CHIP DYNAMIC POWER ESTIMATION ALGORITHM.

Input: standard cell lib, netlist, placement information of design, standard deviation of L and T_{ox} .

Output: analytical expression of the full-chip dynamic power in terms of Hermite polynomials.

1. Build the dynamic power look-up table for each kind of gate $P_{dyn} = f(L, T_{ox}, W_g, C_l)$ under different sets of the four parameters using SPICE simulation.
 2. Build the sub look-up table for the coefficients of Hermite polynomial of dynamic power for each type of gate under different sets of W_g and C_l using the look-up table $P_{dyn} = f(L, T_{ox}, W_g, C_l)$.
 3. Propagate the transition waveforms from primary inputs to the primary outputs based on segment-based analysis method.
 4. Get the coefficients of Hermite polynomials for each gate from the sub look-up table and compute the dynamic power for each gate using (13).
 5. Calculate the analytical expression of the full-chip dynamic power by simple polynomial additions and calculate mean value, standard deviation, PDF and CDF of the dynamic power if required.
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Figure 3: The flow of proposed algorithm.

4.2 Virtual grid based spatial correlation modeling

The new modeling method is based on the observation that the spatial variation in dynamic power of a gate only correlates to its neighboring gates. If we can introduce a new set of uncorrelated variables which can catch the localized correlation, computing the dynamic power of one gate can be done in a constant time by only considering its neighboring gates. Hence total full-chip statistical dynamic power can then be computed by simply adding all dynamic powers at gate-level together in terms of the new set of variables in linear time. The idea is similar to the PCA-based approach but with different set of new independent variables.

Specifically, the chip area is still divided into a set of grid cells. In our case, the grid can be very small so that every grid can even contain one gate. Then we introduce a “virtual” random variable for each grid for one source of process variation.

These virtual random variables are *independent* and will be the basis for statistical dynamic power calculation that concerns spatial correlation. Then we can express the original physical random variable of a gate in a grid as a linear combination of the virtual random variables of its own grid as well as its nearby neighbors. Since each virtual random variable is defined for each grid, which has specific location in a chip, such location-dependent correlation model still retains the important spatial physical meaning (compared to PCA-based models). The grid can be rectangle or hexagonal or other shapes. We use hexagonal grids [4] in this paper since they have minimum anisotropy for 2-D space. And the proposed approach can be applied to any shape-based partition.

Here we define d_c as the grid length. Gates located in the same grid have strong correlation (larger than a given threshold value ρ_{high}) and are assumed to have the same parameter variations. And “spatial correlation distance” d_{max} is defined as the minimum distance beyond which the spatial correlation between any two grids is sufficiently small (or smaller than a given threshold value ρ_{low}) so that we can ignore it.

In this new model, the i^{th} grid is associated with one virtual random variable $\xi_i \sim N(0, 1)$, which is independent of all other virtual random variables. $\Delta L_{intra,i}$ can then be expressed as its k closest neighboring grids. We introduce the concept of *correlation index neighbor set* $T(i)$ for grid i , which defines a set of the indices of ξ_i and their coefficients α_i to model the spatial correlation of $\Delta L_{intra,i}$ as

$$\Delta L_{intra,i} = \sum_{q \in T(i)} \alpha_q \cdot \xi_q. \quad (3)$$

For example, if $T(i)$ for each grid is defined as its closest $k = 7$ neighboring grids, then ΔL located at grid (x_i, y_i) can be represented as a linear combination of seven virtual random variables located in its neighboring set. The grid model are shown in Fig. 4. Take $\Delta L_{intra,1}$ in Fig. 4 for instance, we have $\Delta L_{intra,1} = \alpha_1 \xi_1 + \alpha_2 \xi_2 + \dots + \alpha_7 \xi_7$. This concept of

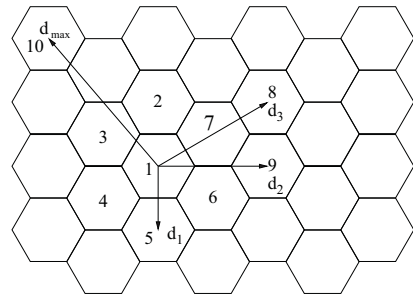


Figure 4: Location-dependent modeling with the $T(i)$ of grid i defined as its seven neighboring cells. correlation index helps to model the spatial correlation. Two

grids close to each other will share more common spatial random variables, which means the correlation is strong. On the other hand, two grids physically far away from each other will share less or no common spatial random variables.

Since $\rho(d)$ is only a function of distance, the number of unique distance values between two correlated grids equals the number of unique element values in $\Omega_{N,N}$. Take the $T(i)$ set we mentioned in Fig. 4 for example. There are only three unique correlation distances d_1 to d_3 . Correspondingly, there are only three unique correlation coefficients in $\Omega_{N,N}$, without including 0 for $d \geq d_{max}$ or $\sigma_{L,intra}^2$ for distance within one grid.

Furthermore, the same correlation index can be used for all grids and the coefficient α_k should be the same for the same distance because of the homogeneousness and isotropy of spatial correlation. For the grid marked 1 in Fig. 4, we only have two unique values among the seven coefficients, i.e., we set $\beta_0 = \alpha_1$, $\beta_1 = \alpha_i, i = 2, 3, \dots, 7$. According to (2), a nonlinear over-determined system can be built to determine the two unique values of β_0, β_1 as follows,

$$\begin{aligned} \beta_0^2 + 6\beta_1^2 &= \sigma_{L,intra}\rho(0) \\ 2\beta_0\beta_1 + 2\beta_1^2 &= \sigma_{L,intra}\rho(d_1) \\ 2\beta_1^2 &= \sigma_{L,intra}\rho(d_2) \\ \beta_1^2 &= \sigma_{L,intra}\rho(d_3) \end{aligned} \quad (4)$$

In matrix form, we can rewrite (3) for whole chip as

$$\Delta L_{intra} = B_{N,N} \cdot \vec{\xi}, \quad (5)$$

where N is the number of grids, and $\vec{\xi} = [\xi_1, \xi_2, \dots, \xi_N]$. According to (3), the correlation index set contains only k neighboring spatial random variables, which is a very small fraction of the total spatial random variables. As a result, $B_{N,N}$ is a sparse matrix. Every gate only relates to k random variables, which has specific location information.

We remark that the new independent spatial correlation model also works for medium and strong correlation cases, which will be shown in the next section.

4.3 Computing gate power by orthogonal polynomials

A random variable $x(\vec{\xi})$ with limited variance can be approximated by truncated Hermite PC expansion as follows [8]:

$$x(\vec{\xi}) = \sum_{q=0}^Q a_q H_q(\vec{\xi}), \quad (6)$$

where $\vec{\xi} = [\xi_1, \xi_2, \dots, \xi_z]$. $\xi_i \sim N(0, 1)$, and are orthogonal to each other. $H_q(\vec{\xi})$ is Hermite polynomial and a_q is the deterministic coefficient. For example, 2nd order Hermite polynomial set includes

$$1, \xi_i, \xi_i^2 - 1, \xi_i \xi_j, (i \neq j). \quad (7)$$

a_q can be determined by

$$a_q = \langle x(\vec{\xi}), H_q(\vec{\xi}) \rangle / \langle H_q^2(\vec{\xi}) \rangle \approx \sum x(\gamma_l) H_q(\gamma_l) w_l, \quad (8)$$

which is a multi-dimensional integration and can be obtained by efficient Smolyak numerical quadrature method. Where γ_l and w_l are Smolyak quadrature abscissas (quadrature points) and weights, respectively [15].

In our problem, $x(\vec{\xi})$ will be the dynamic power for each gate, and eventually for the whole chip. For the j^{th} gate, which is in the i^{th} grid, $\Delta L_{intra,j}$ only relates to k independent virtual random variables in $T(i)$ from (3), and the corresponding variable vector, $\vec{\xi}_{g,j}$, is defined as

$$\vec{\xi}_{g,j} = [\xi_q, q \in T(i), \xi_{ox,i}, \xi_{L,inter}, \xi_{ox,inter}, \xi_{W_g}], \quad (9)$$

in which $\xi_q, \xi_{ox,i}, \xi_{L,inter}, \xi_{ox,inter}$ and ξ_{W_g} stand for the independent variables of the intra-die variation of L_{eff} in

the grid, the intra-die variation of T_{ox} , the inter-die variation of L_{eff} , the inter-die variation of T_{ox} and the glitch width variation of W_g , respectively. The variable vector $\vec{\xi}_{g,j}$ only includes $z = k + 4$ independent variables, where k is the number of closest neighboring grids (See Subsection 4.2).

The dynamic power for one gate (under glitch width W_g with variation and fixed load capacitance C_l) can be presented by Hermite polynomial expansion as

$$P_{dyn,W_g,C_l}(\vec{\xi}_{g,j}) = \sum_{q=0}^Q P_{dyn,q,j} H_q(\vec{\xi}_{g,j}), \quad (10)$$

$P_{dyn,q,j}$ is then computed by the numerical Smolyak quadrature method. In this paper, we use 2nd order Hermite polynomials for statistical dynamic power analysis. The coefficient for q^{th} Hermite polynomial at j^{th} gate, $P_{dyn,q,j}$, can be computed as the following:

$$P_{dyn,q,j} = \sum P_{dyn}(\tilde{\gamma}_l) H_q(\tilde{\gamma}_l) w_l / \langle H_q^2(\vec{\xi}_{g,j}) \rangle, \quad (11)$$

where $\tilde{\gamma}_l$ is Smolyak quadrature sample. From the dynamic power look-up table $P_{dyn} = f(L, T_{ox}, W_g, C_l)$, we can interpolate $P_{dyn}(\tilde{\gamma}_l)$, which is the dynamic power for every Smolyak sampling point.

4.4 Acceleration by building the look-up table

Since we follow the segment-based power estimation method, we have to characterize the powers from the SPICE simulation with different set of parameters. The power of a gate is a function of L and T_{ox} as well as glitch width W_g and load capacitance C_l in the look-up table. $P_{dyn} = f(L, T_{ox}, W_g, C_l)$. We then perform SPICE simulation on different sets of those four parameters to get the accurate data and build the look-up table.

On the other hand, we observe that the coefficients of Hermite polynomials for dynamic power of one gate in (10), (11) are only functions of the type of the gate, ρ_{high} and ρ_{low} (defined in Subsection 4.2) and W_g and C_l . Therefore, another sub look-up table can be used to store the coefficients of Hermite polynomials for each *kind* of gate instead of computing the coefficients for each gate. The time complexity reduces from the number of gates, $O(n)$ to the number of grids, $O(N)$. Fig. 5 shows the flow of sub look-up table construction.

Algorithm: BUILD SUB LOOK-UP TABLE

Input: standard cell lib, ρ_{high} , ρ_{low} , W_g , C_l , $P_{dyn}(L, T_{ox}, W_g, C_l)$

Output: look-up table for coefficients of Hermite polynomials of P_{dyn} under fixed C_l and W_g for each type of gate.

1. Load dynamic power look-up table $P_{dyn} = f(L, T_{ox}, W_g, C_l)$ for each type of gate.
 2. Calculate d_{max}/d_c from ρ_{high} and ρ_{low} to determine the neighboring set. And then solve (4) to determine coefficients in (3).
 3. Generate Smolyak quadrature points set with corresponding weights.
 4. Calculate the coefficients of Hermite polynomials of dynamic power P_{dyn} under fixed C_l and W_g for each type of gate in library.
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Figure 5: The flow of building the sub look-up table.

4.5 Statistical gate power with glitch width variation

To compute the statistical gate power expression considering the glitch width variations, we need to compute the

probability of each switching segment assuming that they follow the normal distribution

$$Pr(w = w_i) = \frac{1}{\sigma_w \sqrt{2\pi}} \exp\left(-\frac{(w_i - \mu_w)^2}{2\sigma_w^2}\right) \quad (12)$$

The Hermite polynomial coefficients for (10) under glitch width w_i and load capacitance C_l can be interpolated from the sub look-up table. For a gate index j with the transition waveform $(p_1, t_1, \sigma_{t1}), (p_2, t_2, \sigma_{t2}), \dots, (p_M, t_M, \sigma_{tM})$, there are $M(M-1)/2$ segments. The resulting statistic power is the probabilistic addition of power from each segments (their Hermite polynomial expressions):

$$P_{dyn,C_l}(\vec{\xi}_{g,k}) = \sum_{i=1}^{M-1} \sum_{j=i+1}^M Pr(i, j) \times P_{dyn,C_l}(\vec{\xi}_{g,k}, i, j) \quad (13)$$

in which $P_{dyn,C_l}(\vec{\xi}_{g,k}, i, j)$ is the dynamic power of gate k caused by the switching segment between transitions E_i and E_j . $Pr(i, j)$ is the probability that the switching segment (E_i, E_j) occurs only if there are transitions at both E_i and E_j , and there are no transitions between E_i and E_j .

$$Pr(i, j) = p_i \times p_j \times \prod_{k=i+1}^{j-1} (1 - p_k) \quad (14)$$

In the following, we write $P_{dyn,C_l}(\vec{\xi}_{g,k})$ as $P_{dyn}(\vec{\xi}_{g,k})$ without confusion.

4.6 Computation of full-chip dynamic power

The dynamic power for each gate are calculated using (13). To compute the full-chip dynamic power, we also need to transfer the local coefficients to corresponding global positions first. Then we can proceed to compute the dynamic power for the whole chip as follows,

$$P_{dyn}^{total}(\vec{\xi}) = \sum_{j=1}^n P_{dyn}(\vec{\xi}_{g,j}). \quad (15)$$

The summation is done for each coefficient of global Hermite polynomials to obtain the analytic expression of the final dynamic power in terms of $\vec{\xi}$. We can then obtain the mean value, variance, PDF and CDF of full-chip dynamic power very easily. For instance, the mean value and variance for the full-chip dynamic power are

$$\mu_{total} = P_{dyn,0th}, \quad (16)$$

$$\sigma_{total}^2 = \sum P_{dyn,1st}^2 + 2 \sum P_{dyn,2nd,type1}^2 + \sum P_{dyn,2nd,type2}^2, \quad (17)$$

where $P_{dyn,ith}$ is the power coefficient for i^{th} Hermite polynomial of second order defined in (7).

5. EXPERIMENTAL RESULTS

We implemented the proposed method and the segment-based analysis [7] in C++ and Matlab V7.8. All the experimental results are carried out in a Linux system with quad Intel Xeon CPUs with 3GHz and 16GB memory. The new method was tested on circuits in the ISCAS'89 benchmark set. The circuits were synthesized with Nangate Open Cell Library under 45nm technology and the placement is from UCLA/Umich Capo [18]. For comparison purposes, we performed Monte Carlo (MC) simulations (10,000 runs) considering spatial correlation, the method in [7] and the proposed method on the benchmark circuits. In our Monte-Carlo implementation, similar to [7], we do not run the SPICE on the original circuits as it is too much time consuming for ordinary computer. Instead we compute the results via interpolation from the characterization data computed from SPICE runs. The 3σ range of L and T_{ox} is set as 20%, of which inter-die variations constitute 20% and intra-die

variations, 80%. L, T_{ox} are modeled as Gaussian random variables. L is modeled as sum of spatial correlated sources of variations based on (2). T_{ox} is modeled as an independent source of spatial variation. The same framework can be easily extended to include other parameters of variations.

The characterization data for each type of gate in standard cell library is collected using HSPICE simulation. For each type of gate, we perform repeat simulation on sampling points in the 3σ range of L, T_{ox} and input glitch width W_g for several different load capacitances to obtain the gate dynamic powers and gate delays. The table of characterization data will be used to interpolate the value of dynamic power for each type of gate with different process parameters. We use 21 sample points for glitch width, from 50ps to 150ps.

In transition waveform computation, the gate delays are obtained through the table of characterization data and the input signal probabilities are 0.5, with switching probabilities of 0.75. The test cases are given in Table 1 (all length units in μm). In the first column, s and w stands for strong and weak spatial correlations, respectively.

Table 1: Summary of benchmark circuits.

Testcase	Gate #	Grid #	Area
s1196 (s)	529	27	95×90
s1196 (w)	529	294	95×90
s5378 (s)	2779	93	209.5×198
s5378 (w)	2779	1300	209.5×198
s9234 (s)	5597	161	278.5×270
s9234 (w)	5597	2358	278.5×270

The comparison results of mean value and standard deviations of full-chip dynamic power are shown in Table 2, where *MC Co* represent Monte Carlo considering spatial correlation, and *New* is the proposed method. The method in [7] can not consider spatial correlation as it assumed that the power for the gates are independent gaussian random variables. In implementation of [7], we assume the same variation for L_{eff} and T_{ox} but without spatial correlations. The average errors for mean and standard deviation (σ) values of the *New* technique are 1.49% and 6.54% compared to *MC Co*, respectively. While for the method in [7], the average errors for mean value and σ are 3.04% and 96.97%, respectively. As a result, without considering spatial correlations can lead to significant errors. Further more, from the comparison between mean and standard deviation of *MC Co*, the average *std/mean* is 7.21% which means spatial correlation in process parameter has significant impact on the distribution of dynamic power. The results in Table 2 also show that our method can handle both strong and weak spatial correlations by adjusting grid size.

Table 3: CPU time comparison.

Test Case	CPU time (s)			Speedup Over	
	MC Co	[7]	New	MC Co	[7]
s1196 (s)	1261	12	0.30	4242	42
s1196 (w)	1225	13	0.33	3743	40
s5378 (s)	7037	74	1.19	5927	62
s5378 (w)	6859	73	1.41	4874	52
s9234 (s)	14805	151	2.11	7026	71
s9234 (w)	13978	151	2.84	4927	53

Table 3 compares the CPU times of three methods, which shows that the *New* method is much faster than the method in [7] and MC simulation. On average, the proposed technique has about 53X speedup over [7] and 5123X speedup over the MC method. In [7], the dynamic power of each gate needed to be interpolated from the look-up table due to different L, T_{ox} and glitch width value variations, the complexity is a linear function of the number of gates $O(n)$, however, in *New* algorithm, only the coefficients of Hermite polynomials for each type of gate are needed to compute and

Table 2: Statistical dynamic power analysis accuracy comparison against Monte Carlo.

Test Case	Grid #	Mean Value (mW)			Errors		Standard Deviation (mW)			Errors	
		MC Co	[7]	New	[7]	New	MC Co	[7]	New	[7]	New
s1196 (s)	27	1.14	1.19	1.14	3.82%	0.49%	0.0912	0.00394	0.0845	95.68%	7.33%
s1196 (w)	294	1.14	1.19	1.14	3.98%	0.41%	0.0671	0.00395	0.0645	94.11%	3.94%
s5378 (s)	93	6.09	6.24	5.98	2.46%	1.85%	0.470	0.00877	0.435	98.13%	7.61%
s5378 (w)	1300	6.09	6.23	5.98	2.29%	1.85%	0.436	0.00891	0.412	97.96%	5.68%
s9234 (s)	161	12.8	13.2	12.5	2.94%	2.31%	0.964	0.0185	0.882	98.08%	8.52%
s9234 (w)	2358	12.8	13.1	12.5	2.78%	2.14%	0.894	0.0191	0.839	97.87%	6.14%

the overall complexity is a linear function of the number of grids $O(N)$.

6. CONCLUSION

In this paper, we have proposed a new statistical dynamic power estimation method considering the spatial correlation in the presence of process variation. The new method considers the variational impacts of channel length on gate dynamic powers. To consider the spatial correlation, we adopt a newly proposed spatial correlation model where a new set of uncorrelated variables are defined over virtual grids to represent the original physical random variables by least-square fitting. To compute the statistical dynamic power of a gate on the new set of variables, the new method applies the flexible orthogonal polynomials based method, which can be applied to any gate models. We adopted the segment-based statistical power method to consider the impacts of glitch width variations on dynamic power. The total full chip dynamic power expressions are then computed by summing up the resulting orthogonal polynomials (their coefficients) on the new set of variables for all gates. Experimental results on ISCAS'89 benchmark with 45nm technology show that the proposed method has about 53X speedup over recently proposed segment-based statistical power estimation method [7] and many orders of magnitudes over the Monte Carlo method.

7. REFERENCES

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