Symbolic Macromodeling for Statistical Simulation of Operational Amplifiers

Lanlan Dong, Guoyong Shi, and Jiandong Cheng

***Abstract*—Symbolic circuit simulator is traditionally applied to small-signal analysis of analog circuits. This paper establishes a symbolic behavioral macromodeling method applicable to both small-signal and large-signal analysis of general two-stage operational amplifiers (op-amps). The proposed method creates a two-pole parametric macromodel whose parameters are analytical functions of the circuit element parameters generated by a symbolic circuit simulator. A moment matching technique is used in deriving the analytical model parameter. The created parametric behavioral model can be used for op-amp performance simulation in both frequency and time domains. In particular, the parametric models are highly suited for fast statistical simulation of op-amps in the time-domain. Experiment results show that the statistical distributions of the op-amp slew and settling time characterized by the proposed model agree well to the transistor-level results in addition to achieving significant speedup.**

***Index Terms*— Analog behavioral model, large-signal analysis, moment matching, operational amplifiers (op-amps), process variation, statistical analysis, symbolic analysis.**

1. Introduction

The art of operational amplifier (op-amp) macromodeling has been a constantly studied research subject since the beginning of monolithic integrated circuit (IC) op-amps [1]. The two-pole macromodel shown in Fig. 1 has been widely used in the literature for small-signal analysis of two-stage amplifiers [2]. Some early works [3], [4] adapted the two-pole model by incorporating nonlinear devices (transistors or diodes) in order to characterize the large-signal transient behaviors. Obviously, these models take different forms in the frequency and time domains.

In 1982 Chuang proposed a second-order behavioral model (Fig. 2) for behavior analysis of slewing and settling of two-stage op-amps [9]. The model consists of a current limiter in the feedforward path which reflects the current limiting effect by some transistor in the op-amp. The block denoted by $H(s)$ is the two-pole model shown in Fig. 1.

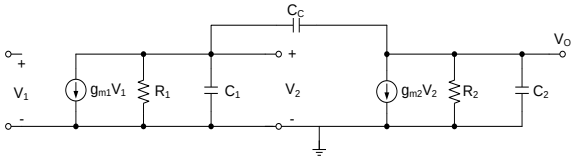

Fig. 1. Two-pole macromodel for a two-stage op-amp.

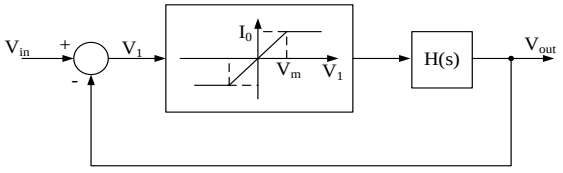

Fig. 2. Chuang's behavioral model for transient analysis [9].

For an instant step input, the voltage input to the current limiter is large and the current limiter in Fig. 2 is in saturation when the output starts to slew. During this period the feedback loop is virtually not in effect. As the output waveform settles to the vicinity of the final value, the current limiter enters the linear operation and the feedback loop becomes effective, and the settling behavior is governed by a linear system.

Several works have attempted to improve Chuang's model from a variety of aspects, such as Lin and Nevin [10] for smooth transition from slewing to settling, Wang and Harjani [11] for improved slew rate formula when more advanced technology is used, and Yavari et al. [12] for the case when the op-amp output stage is limited to low-current operation. The different slew rate formulas proposed only apply to circuits with the assumed working conditions, lack the generality for use in design automation tools.

The recent work [13] developed a unified formulation for slew and settling analysis by adapting Chuang's two-pole model into a symbolic setting. However, in that work the second-order linear block $H(s)$ is constructed by

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extracting approximate poles, it does not have the circuit-form representation as shown in Fig. 1.

This paper is a continuation of the work [13] by proposing a new symbolic construction of the behavioral model which takes the behavioral circuit-form shown in Fig. 1. The advantage of maintaining a macromodel in circuit form is that it can be extended easily to multiple-stage op-amp designs because the building blocks used in Fig. 1 are standard. By inserting such a symbolic model in the Chuang's behavioral configuration shown in Fig. 2, both small-signal and large-signal op-amp performance characteristics can be evaluated by behavioral simulation. Moreover, the proposed macromodel can be used for fast Monte Carlo characterization of the op-amp slew and settling behavior, which was not studied in [13]. Process variation is currently one of the major issues that affect the yield and product quality of nanometer integrated circuits. Statistical verification of analog ICs has been the subject of some recent publications, such as techniques on Monte Carlo sampling [5], and using symbolic methods to predict the circuit response variations in the frequency and time domains [6]-[8].

The proposed symbolic macromodeling method is developed in section 2. Experimental validation of the accuracy and speed of the proposed model for statistical simulation is presented in section 3. This paper is concluded in Section 4.

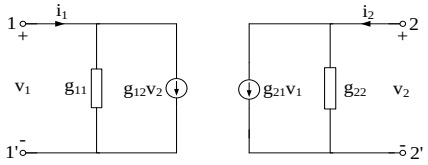
2. Symbolic Modeling Method

2.1 Two-Port Admittance Model

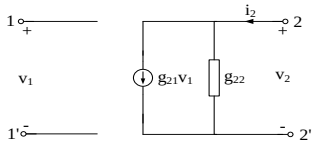
A multi-stage op-amp circuit is composed of several two-port stages, each stage can be described by the following 2x2 small-signal admittance equation

$$\begin{pmatrix} i_1 \\ i_2 \end{pmatrix} = \begin{pmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix}, \tag{1}$$

where the four admittance parameters correspond to those shown in Fig. 3(a). The input conductance g_{11} is usually very small (or impedance very high) for MOS op-amps; hence, the input port can be assumed open. In this work we use the simplified two-port model shown in Fig. 3(b). Note that the two-stage macromodel shown in Fig. 1 consists of two stages of such simplified two-port models.



(a) Two-port circuit model.



(b) Simplified two-port circuit model.

Fig. 3. Two-port circuit models.

2.2 Symbolic Model Generation

Assume that a circuit block with one input and one output has a rational transfer function in the following *s*-expanded form:

$$H(s) = \frac{N(s)}{D(s)} = \frac{b_0 + b_1 s + b_2 s^2 + \ldots + b_q s^q}{a_0 + a_1 s + a_2 s^2 + \ldots + a_r s^r}. \tag{2}$$

With a symbolic tool, this function can be derived in the form that all the coefficients b_j's and a_k's in (2) are analytical functions of the small-signal parameters of the corresponding circuit block [14], [15]. When the circuit parameters change, the values of these coefficients can be computed accordingly without carrying out a new construction.

Suppose that $H(s)$ is in admittance form. Let the Taylor expansion of $H(s)$ at $s = 0$ be,

$$\hat{H}(s) = m_0 + m_1 s + m_2 s^2 + \ldots, \tag{3}$$

where the coefficients m_k are called *moments* [16].

The two admittance parameters given in the two-port schematic in Fig. 3(b) have the following forms

$$g_{21} = g_m, \tag{4a}$$

$$g_{22} = \frac{1}{R} + Cs, \tag{4b}$$

where g_m is a transconductance, R is a resistive load, and C is a capacitive load. These two expressions are already in the *s*-expanded forms of the 0^{th} and 1^{st} orders. The coefficients can be determined by matching the coefficients to (3).

Assume that an op-amp is of finite dc-gain, i.e., $a_0 \neq 0$. Then by moment-matching equations (2) and (3), we have

$$m_0 = \frac{b_0}{a_0} \tag{5a}$$

$$m_1 = \frac{b_1 - m_0 a_1}{a_0} \tag{5b}$$

Since the coefficients a_0, a_1, b_0 and b_1 are symbolic functions of the circuit small-signal parameters, so are the moments m_0 and m_1. Consequently, the parameters g_{m1}, g_{m2}, R_1 , R_2, C_1 and C_2 appearing in the two-pole macromodel in Fig. 1 can be derived as analytical functions of the small-signal parameters of the original op-amp circuit.

We emphasize again that such symbolic construction is

carried out only once for any given circuit. The constructed behavioral model can be used repeatedly for statistical computation provided that the small-signal parameter values are updated when necessary. The proposed macromodeling steps are summarized below.

Symbolic Macromodeling Steps

Step 1: Given a multi-stage op-amp, use the final value of the step input for simulating the dc operating point and generating the small-signal circuit parameter values (it is usually an HSPICE simulation.)

Step 2: Partition the circuit into several cascaded two-port blocks. Remove the biasing and feedback parts of circuit if necessary.

Step 3: Use a symbolic ac analysis tool to obtain the port transadmittances of each stage. Use the formulas given in (5a) and (5b) to determine the moments m_0 and m_1. Use equation (4a) and (4b) to determine the macromodel parameters.

Step 4: Place back the feedback compensation elements (e.g., capacitor C_C and the nulling resistor R_C if needed) in the macromodel.

2.3 Use of the Macromodel

Both the current limiter and the second-order $H(s)$ model in Fig. 2 (i.e., the Chuang's behavioral model) can be described in standard HSPICE netlist. In HSPICE, the current limiter can be described by a G element with saturation [17]

G in+ in- NC+ NC- MAX = I_0 MIN = - I_0 g_{m1}

Replacing the transconductance g_{m1} in the two-pole model (Fig. 1) by the current limiter G just defined, we get the behavioral model shown in Fig. 4, where the current limiter is embedded in the two-stage model $H(s)$.

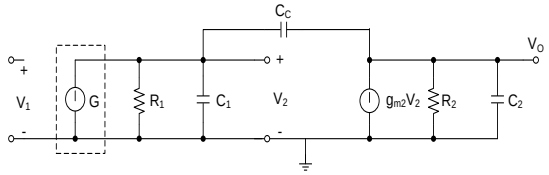


Fig. 4. Two-stage behavioral model containing a current limiter G.

3. Experimental Results

Two op-amp circuits were used to validate the accuracy and efficiency of the proposed modeling method. The TSMC 0.18μm technology was used for simulation. Circuit A (Fig. 5) is a simple two-stage op-amp and Circuit B (Fig. 6) is a rail-to-rail folded-cascode op-amp. We shall show the simulation results in both frequency-domain and time-domain. To demonstrate the robustness of the proposed models, we also changed the circuit working conditions. For example, the supply voltages are different for the two circuits. In the transient simulations the op-amps are connected as a voltage follower (Fig. 7).

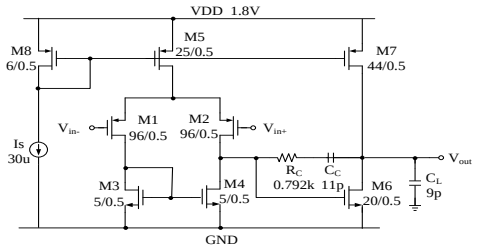


Fig. 5. Circuit A: a simple two-stage operational amplifier.

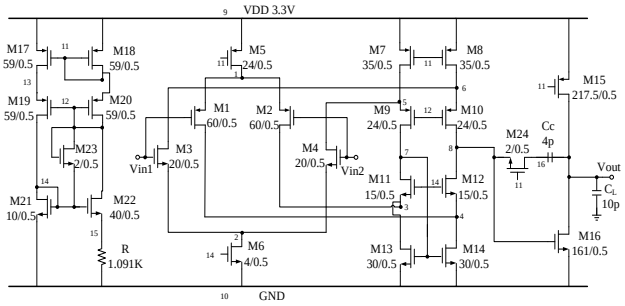


Fig. 6. Circuit B: a rail-to-rail folded-cascode amplifier.

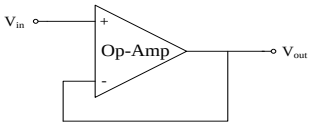


Fig. 7. Voltage follower.

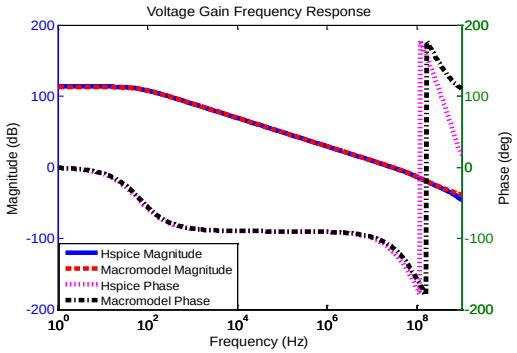


Fig. 8. Comparison of the frequency responses for Circuit B.

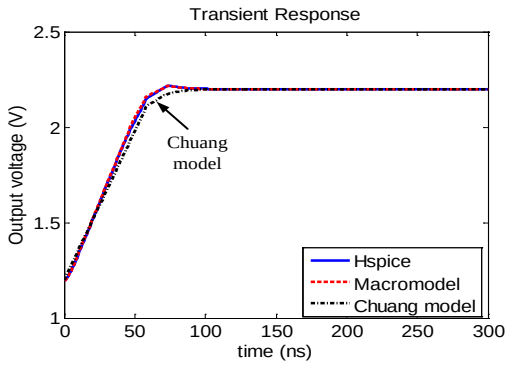


Fig. 9. Comparison of the transient responses of Circuit B.

Fig. 8 shows the frequency responses of Circuit B by using the macromodel and HSPICE; the results agree very well. Fig. 9 shows the transient step responses of Circuit B

by using the two macromodels (the proposed symbolic model and Chuang's non-symbolic model) and HSPICE. Except for the slight deviation by using Chuang's non-symbolic model, the waveform produced by the symbolic macromodel agrees very well to that of HSPICE. Similar results were observed for Circuit A.

As pointed out by Yavari et al. in [12], the classical slew rate formula (also used in the Chuang's model) was not accurate for low-current operation. Hence, it is of interest to examine whether the proposed behavioral model can predict accurate slew rates in different circuit operating conditions. Shown in Fig. 10 is a comparison of the slew rates of Circuit A measured by the three different models. The supply current was adjusted by adjusting the width of the transistor M7 from 38μm to 60μm. The curves show that our symbolic macromodel estimated the slew rate as accurate as the HSPICE transistor-level simulation results for different supply currents, whereas Chuang's model failed to predict the correct slew rates when the current level is low. This test testifies that the proposed symbolic behavioral model is more robust to varying operating conditions.

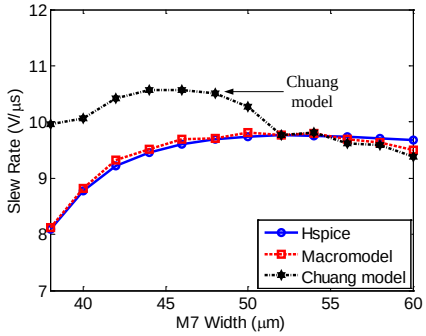


Fig. 10. Comparison of the slew rates of Circuit A computed by the three methods with respect to the size of M7.

Reported next are the statistical simulation results tested for the transient response of Circuit B by varying the compensation capacitor C_C. In the experiment the values of C_C were sampled by a normal distribution with the mean μ = 4pF and the standard variance δ = 1/3pF, with the maximum absolute variation truncated at 1pF (i.e., 3δ = 1pF by the HSPICE *agauss* command.)

Plotted in Figs. 11 and 12 are the Monte Carlo slew rate and settling time results of 10,000 samples by using the proposed macromodel and HSPICE. The accurate agreement is further justified by the scatter plots shown in Fig. 13. It tells us that the statistical variation of the feedback capacitive compensation can be very accurately characterized by the proposed method. Finally, Fig. 14 shows that using the macromodel for statistical simulation is more advantageous in speed than running repeated HSPICE simulations.

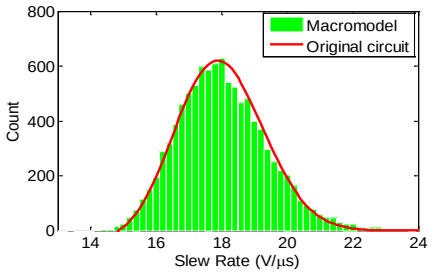


Fig. 11. Comparison of slew rate distribution for Circuit B.

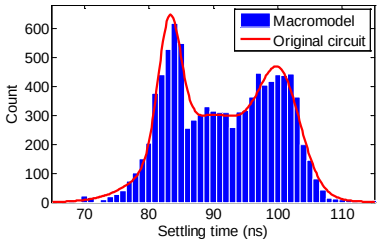


Fig. 12. Comparison of settling time distribution for Circuit B.

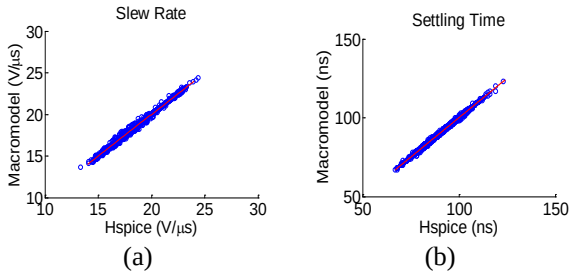


Fig. 13.Scatter plots of the data shown in Figs. 11 and 12: (a) slew rate, (b) settling time.

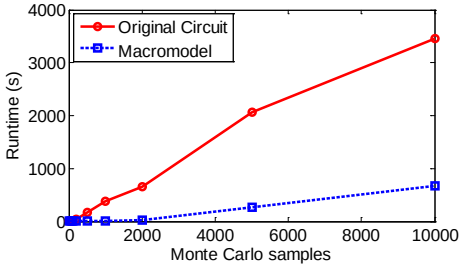


Fig. 14. Monte Carlo runtime comparison for Circuit B.

4. Conclusion

A symbolic behavioral modeling method has been proposed for general multiple-stage operational amplifiers. The feature of symbolic model parameters can facilitate the simulation of varying circuit operating conditions, which is advantageous for statistical analog circuit verification. The experimental results have specifically demonstrated that the proposed model can be used efficiently to predict the large-signal behavior of op-amps in the time-domain, which has hardly been addressed in the open literature.

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