A PSpice Tutorial

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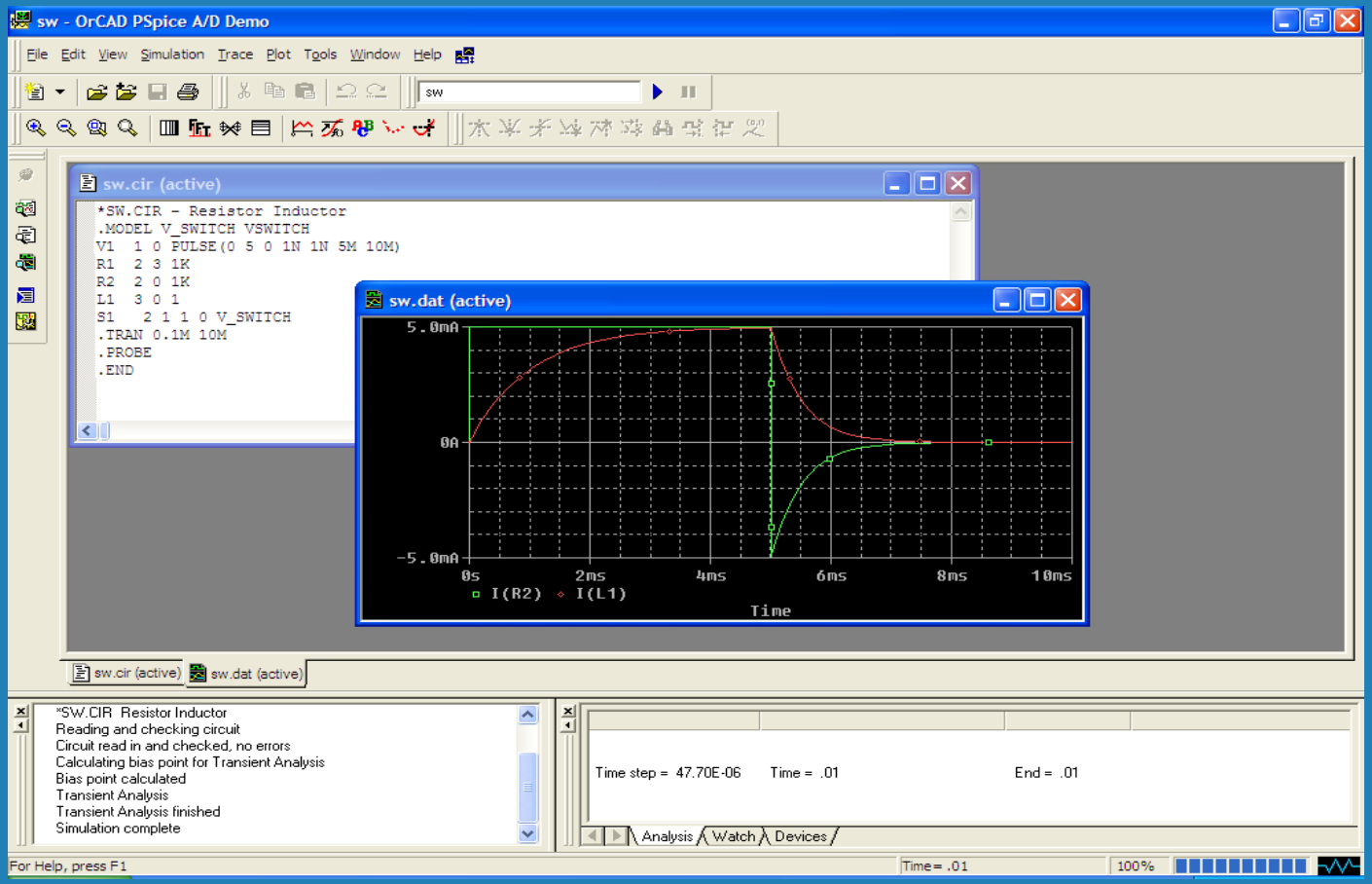
History

- SPICE – Simulation Program with Integrated Circuit Emphasis
- Developed by University of California at Berkeley starting mid-1970s
- In 1984 MicroSim Corporation (now Cadence) made SPICE available for PC under the name PSpice.

OrCAD PSpice

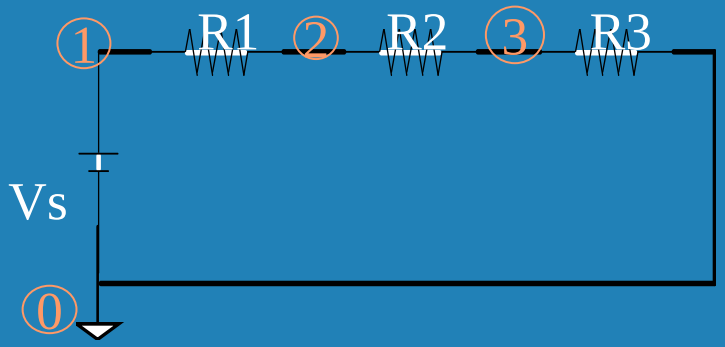


Free Download

- PSpice Demo version can be downloaded (free) from www.orcad.com
- My OrCAD_Demo version was installed in C:\Program Files\OrCAD_Demo\
- For model library, add the line in netlist:

  .lib “nom.lib”

Example – DC Analysis



The first line is always a comment.

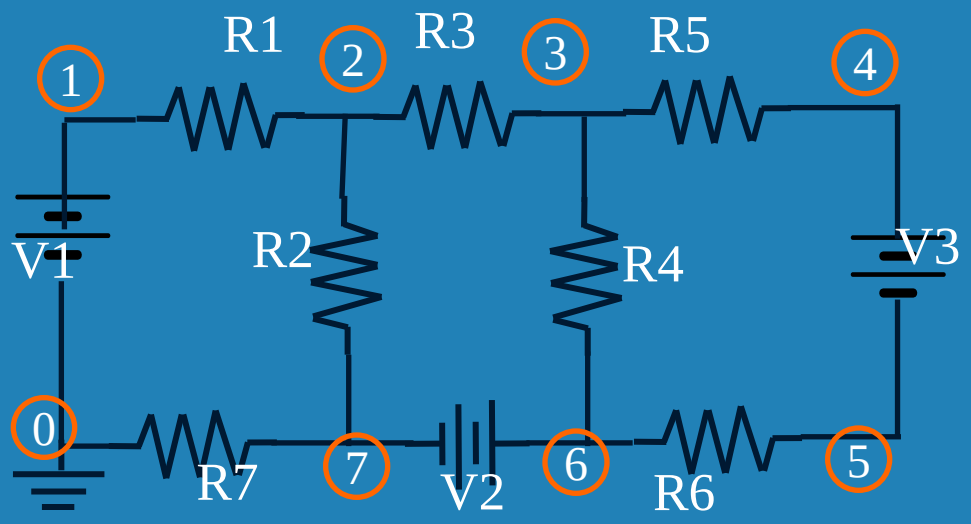
```
*DC1.CIR – SERIES CIRCUIT
VSOURCE  1  0  5
R1  1  2  1K
R2  2  3  2K
R3  3  0  3K
.DC   VSOURCE  6  6  1
.PRINT DC V(2,3) V(2) I(R2)
.END
```

start end inc (>0)

Example

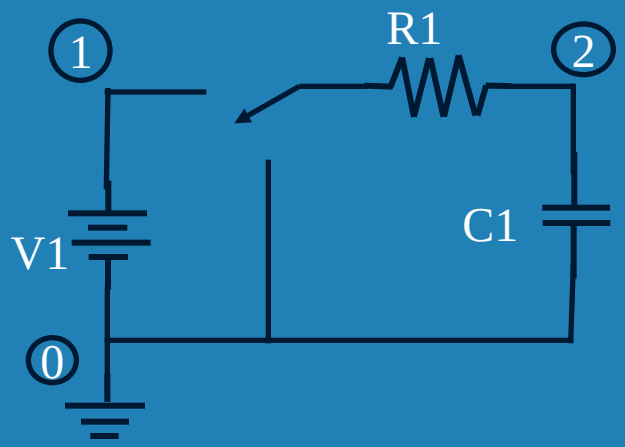
```
*DC2.CIR – SERIES CIRCUIT
VSOURCE  1  0  5
R1  1  2  1K
R2  2  3  2K
R3  3  0  3K
.DC   VSOURCE  5 10 0.5
* DC analysis from 5 to 10 volts, step 0.5 volts.
.PRINT DC V(2,3) V(2) I(R2)
.PROBE
* Use graphics – a comment line
.END
```

Example




```
*DC4.CIR
V1  1 0 5
V2  6 7 8
V3  4 5 10
R1  1 2 100
R2  2 7 200
R3  2 3 300
R4  3 6 400
R5  3 4 500
R6  5 6 600
R7  7 0 700
.DC V1  5 5 1
.PRINT DC I(R4)
.END
```

Example – Transient Analysis



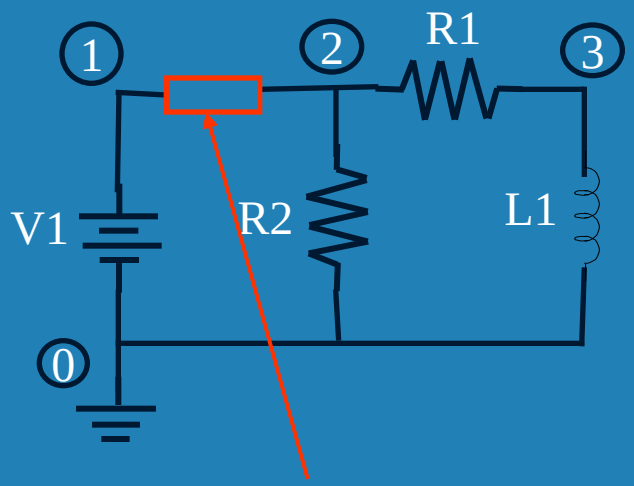

```
*TR1.CIR – Resistor Capacitor
V1  1 0 PULSE(0 5 0 1N 1N 5M 10M)
R1  1 2 1K
C1  2 0 1U
.TRAN 1M 10M
.PROBE
.PRINT TRAN V(2) V(1,2) I(R1)
.END
```

time step

duration

PULSE([low] [high] [delay] [rise] [fall] [duty] [period]**)**

Switch Model



Voltage Controlled Switch (V1 high – ON, V1 low – OFF)

```
*SW.CIR – Resistor Inductor
.MODEL V_SWITCH VSWITCH
V1  1 0 PULSE(0 5 0 1N 1N 5M 10M)
R1  2 3 1K
R2  2 0 1K
L1  3 0 1
S1   2 1 1 0 V_SWITCH
.TRAN 0.1M 10M
.PROBE
.END
```

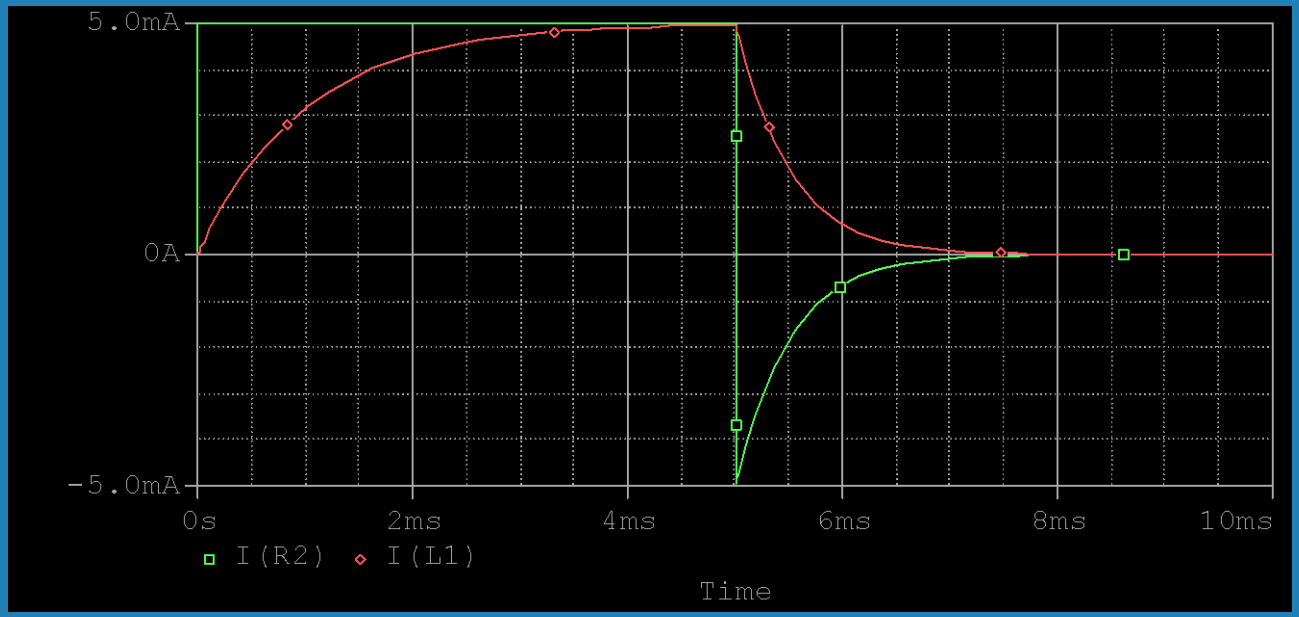
Model name

Model type

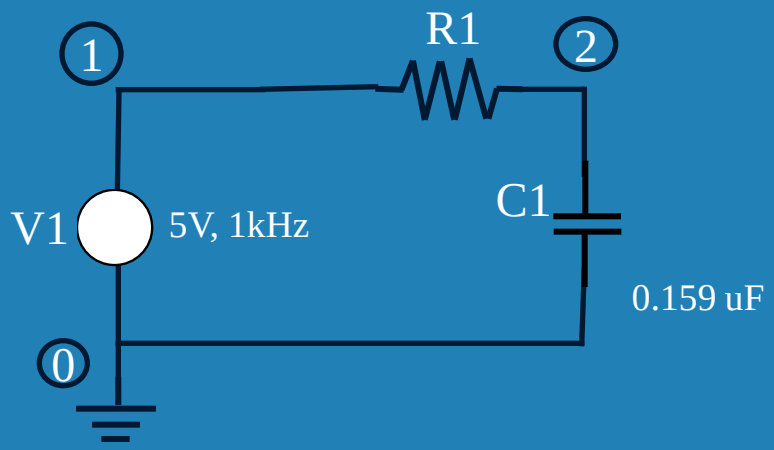
Controlled by

Simulation Result

SW.CIR



Example – AC Analysis



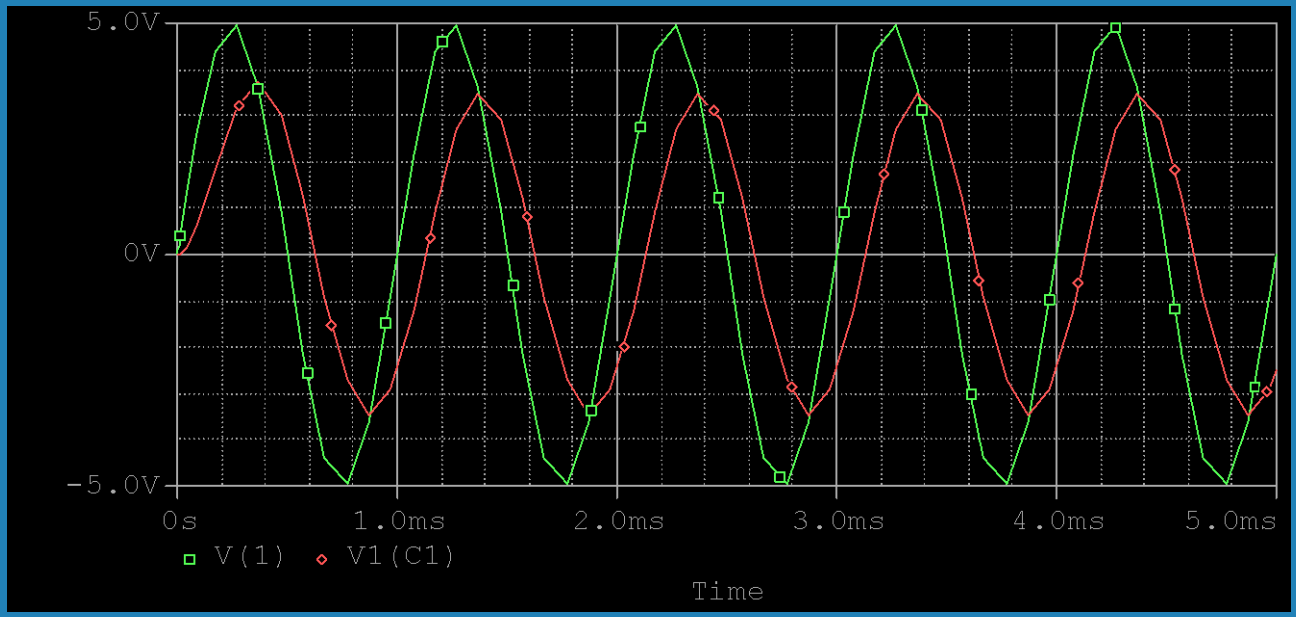
$1/(2\pi fC) = 1K\Omega$

```
*AC1.CIR – AC SOURCE
V1  1 0 SIN(0 5 1000)
R1  1 2 1K
C1  2 0 .159U
.TRAN .1M 5M
.PRINT TRAN V(1) V(1,2) V(2)
.PROBE
.END
```

SIN([DC_offset] [amplitude] [freq] [delay] [damping_factor] [phase])

Simulation Result

AC01.CIR



Note the 45 degree phase shift.

Output syntax

.TRAN 0.1M 5M 4M 0.01M

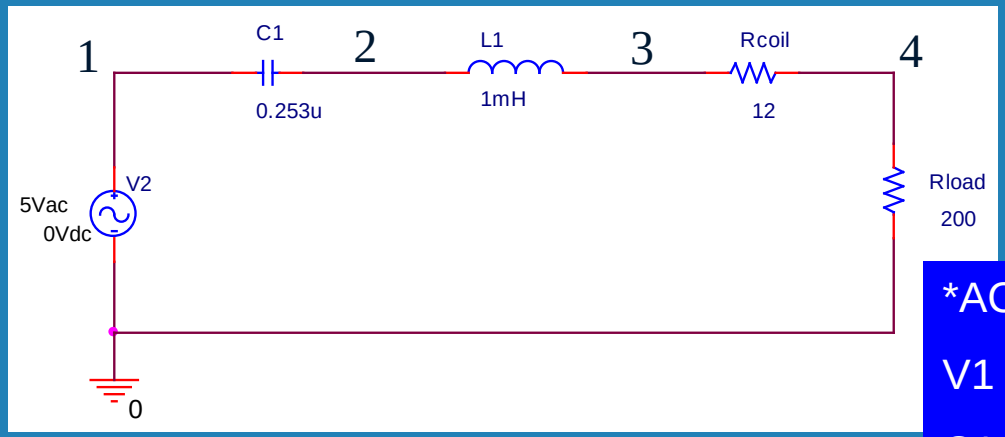
No print until 4M. Refined time-step 0.01M.

.PRINT DC V(4) V(5,6) I(Vsource)

The current output variable has the form I(Vname).

For PSPICE, it can be I(Rname).

Example – Frequency Sweep



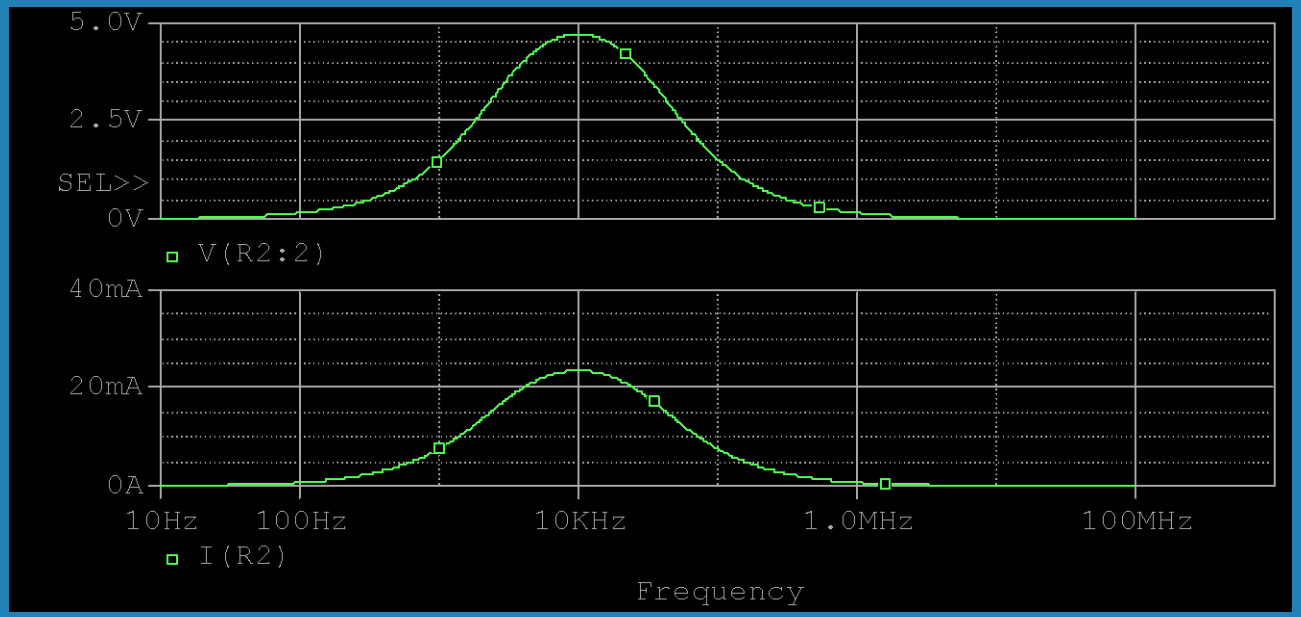
Decade scale (log)

.AC DEC [pts] [low_f] [hi_f]

```
*AC5.CIR – RESONANT
V1  1 0 AC 5
C1  1 2 0.253U
L1  2 3 1M
RCOIL  3 4 12
RLOAD 4 0 200
.AC DEC 100 10 100MEG
.PROBE
.END
```

Simulation Result

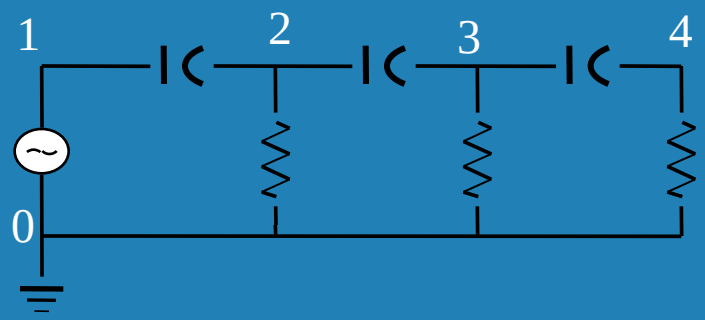
AC5.CIR



V4

I(RLOAD)

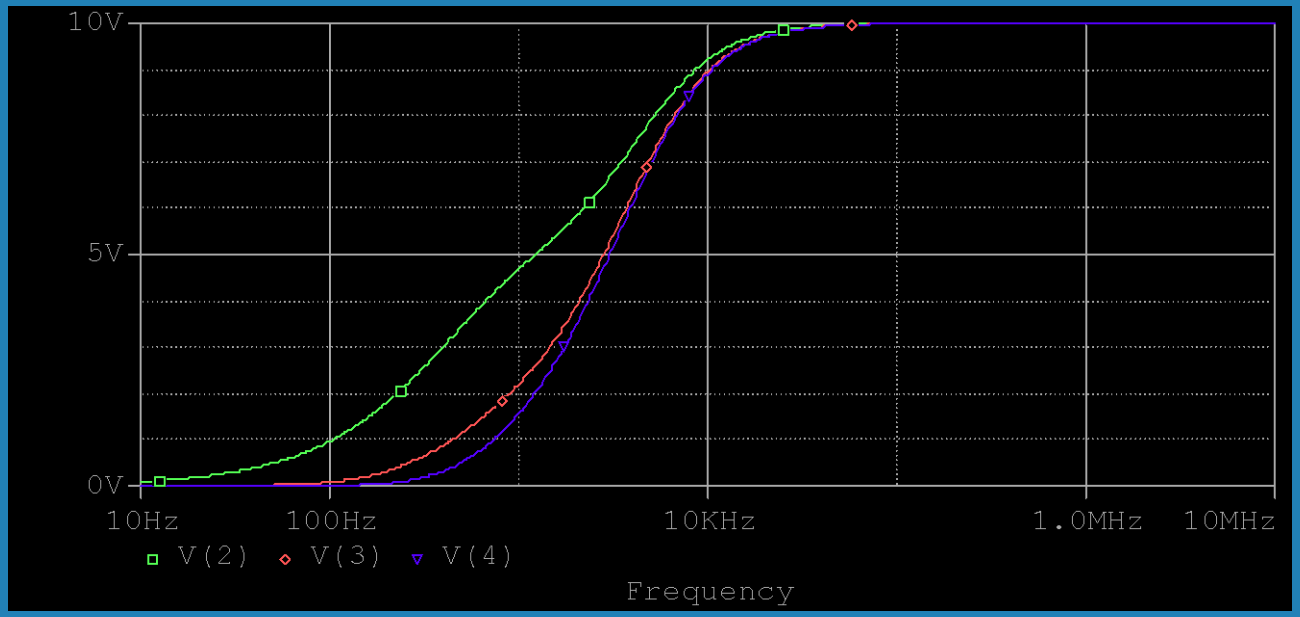
High-Pass Filter




```
*AC8.CIR - Multi-stage high pass circuit
Vs 1 0 AC 10
C1 1 2 0.159U
C2 2 3 0.159U
C3 3 4 0.159U
R1 2 0 1K
R2 3 0 1K
R3 4 0 1K
.AC DEC 100 10 10MEG
.PROBE
.END
```

Result

AC8.CIR

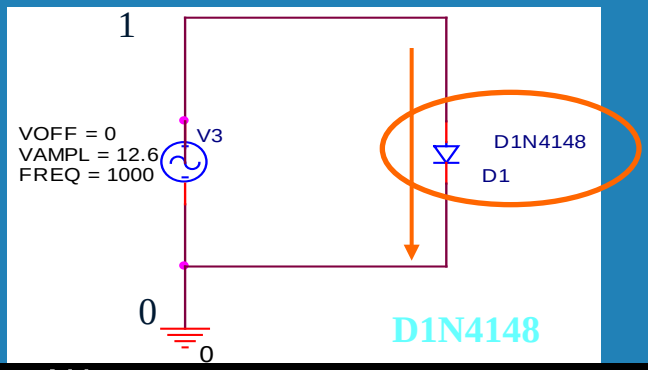


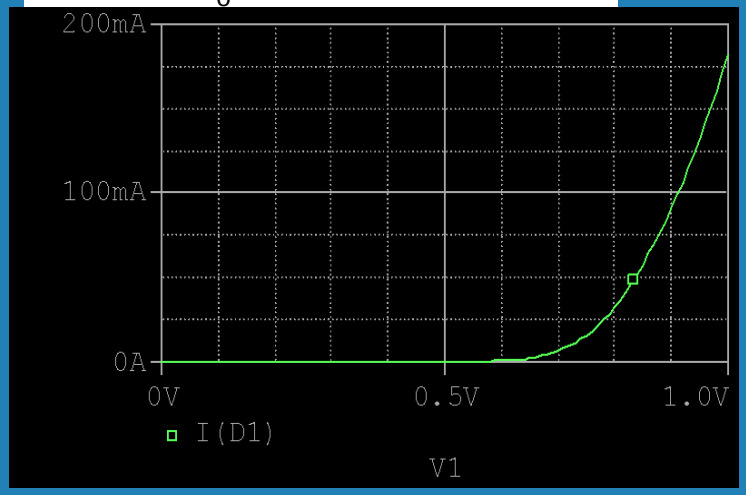
Electronic Circuitry

- The writers of PSpice have created libraries of diodes, op amps, and transistors.
- In the evaluation version of PSpice, there is only one library. All diodes, op amps, and transistors have been modeled in EVAL.LIB.

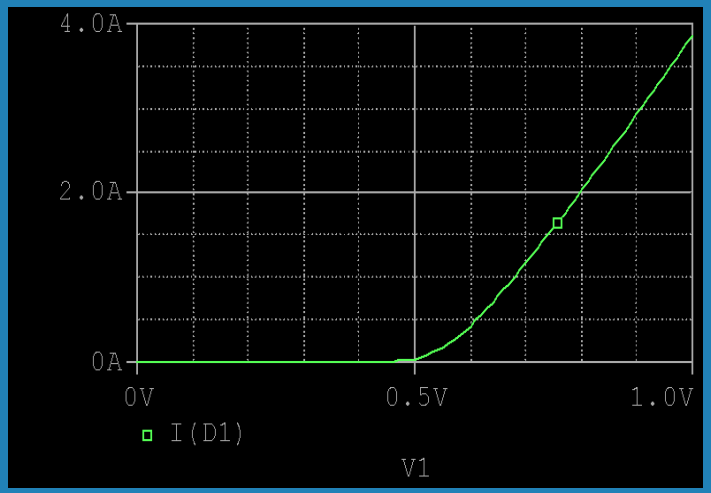
Diode

```
*DIODE00.CIR -- 1N4148 DIODE TEST
.LIB "NOM.LIB"
V1 1 0 5
*D1 1 0 D1N4148
D1 1 0 MBD101
.DC V1 0 1 0.01
.PROBE
.END
```

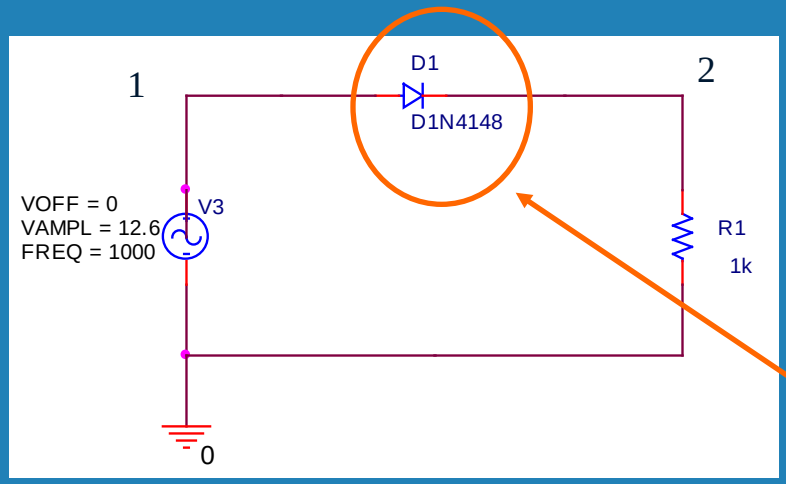




MBD101



Diode



*DIODE01.CIR -- Half wave rectifier

.lib "nom.lib"

V1 1 0 SIN(0 12.6 1000)

D1 1 2 **D1N4148**

R1 2 0 1K

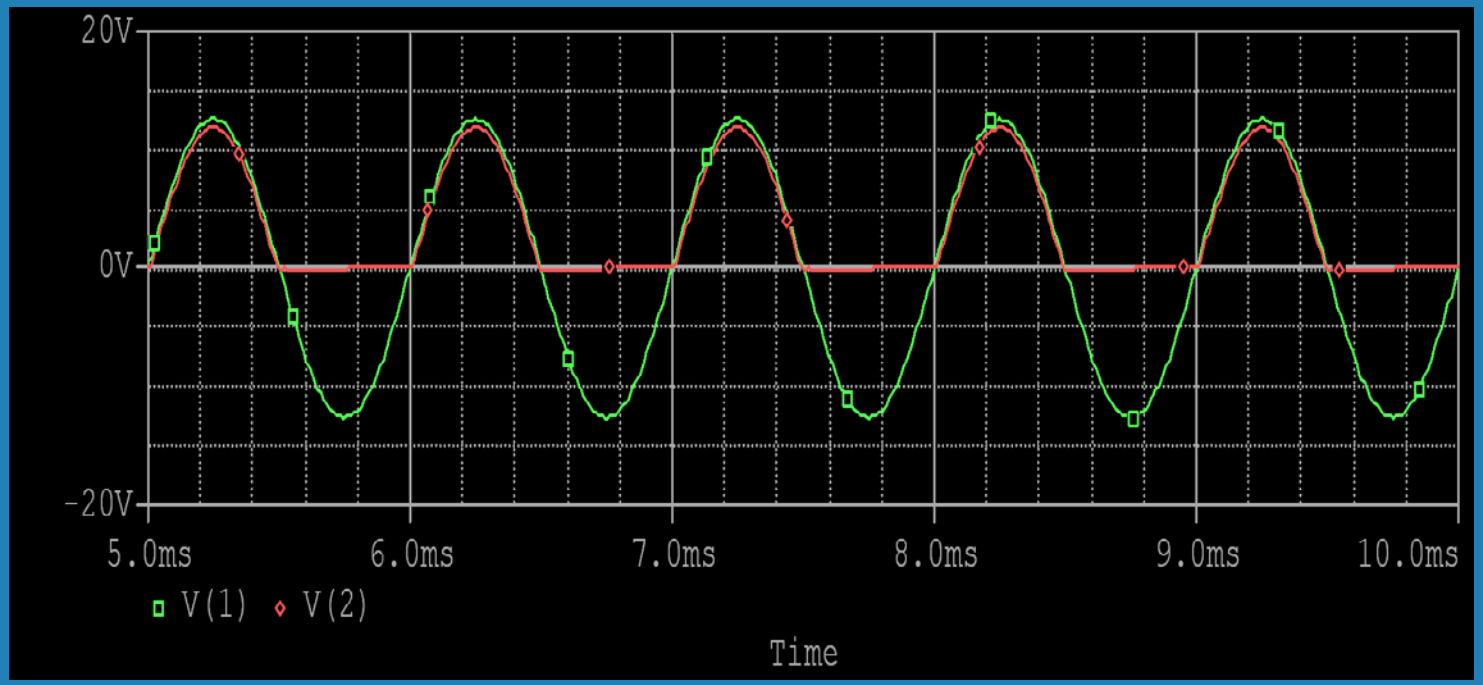
.TRAN 0.1M 10M 5M 0.01M

.PROBE

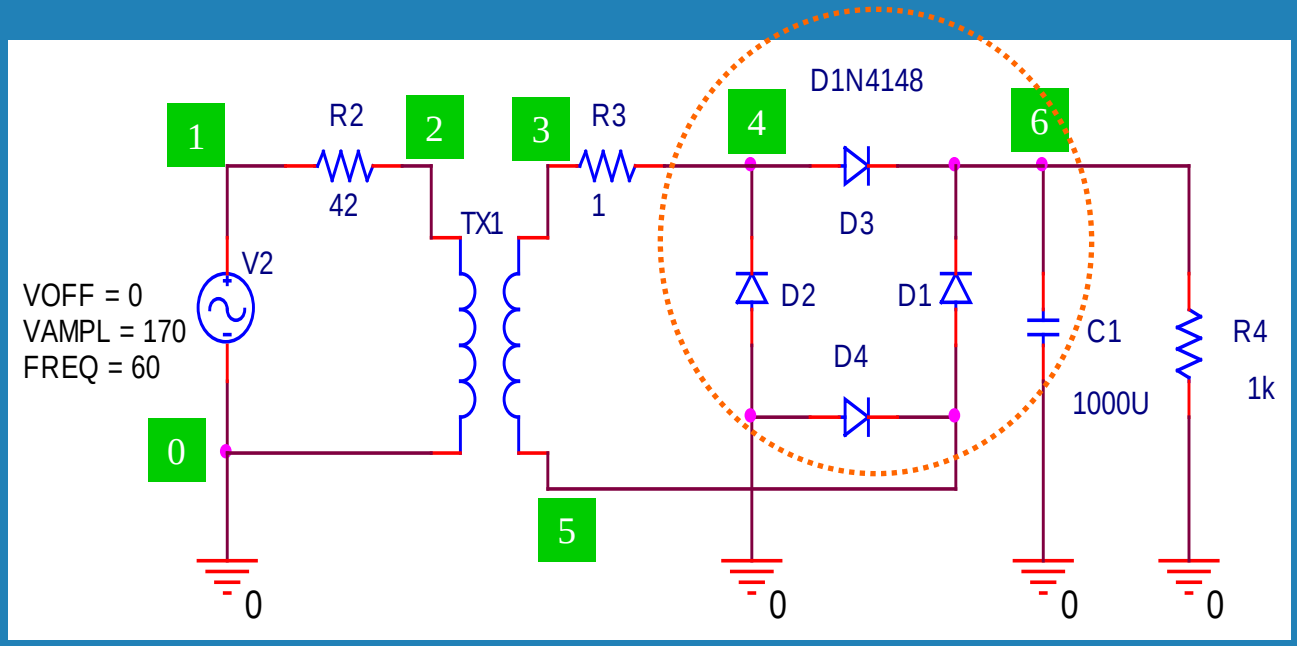
.END

Simulation

DIODE01.CIR



Bridge Rectifier



Rectifier Netlist

*RECTIFIER.CIR -- Full wave rectifier with filter

.lib "nom.lib"

V1 1 0 SIN(0 170 60)

Rprimary 1 2 42

Lprimary 2 0 2

Rsecondary 3 4 1

Lsecondary 3 5 0.0221

K1 Lprimary Lsecondary 0.999

D1 4 6 D1N4148

D2 0 4 D1N4148

D3 0 5 D1N4148

D4 5 6 D1N4148

C1 6 0 1000U

RLOAD 6 0 1K

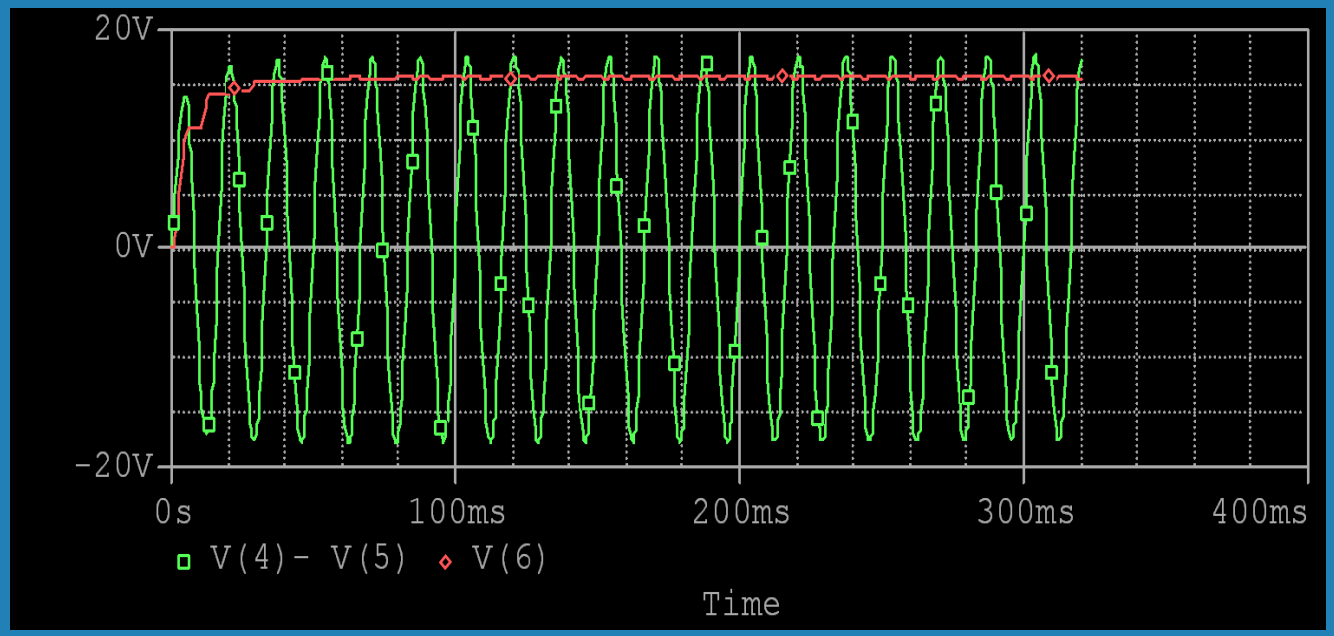
.TRAN 0.016 0.32 0 0.60M

.PROBE

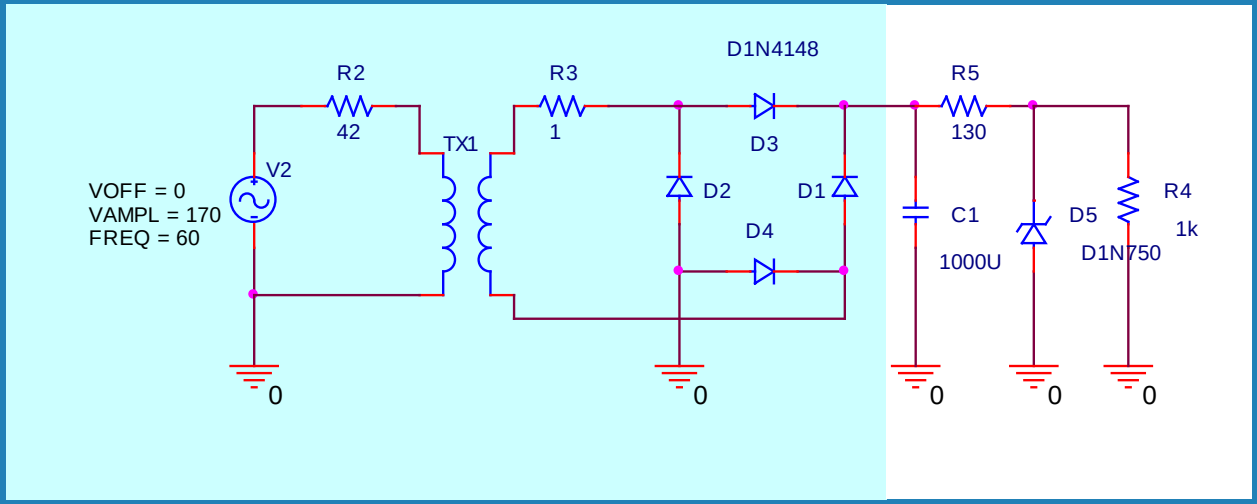
.END

Simulation Result

RECTIFIER.CIR

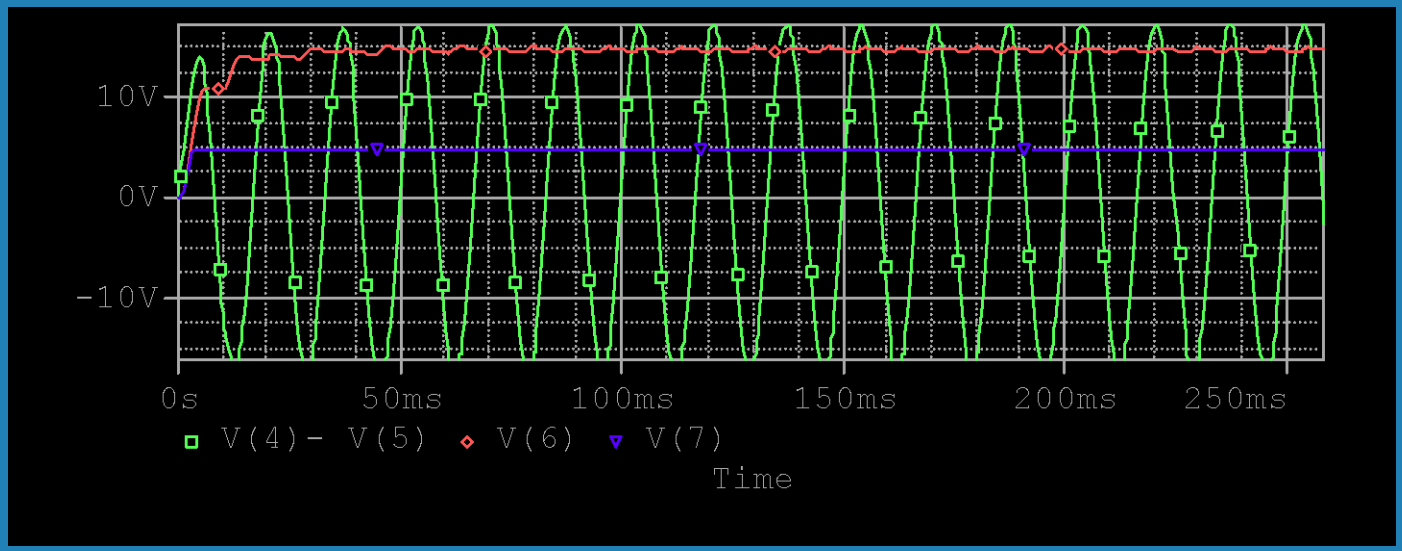


A Zener Diode Added

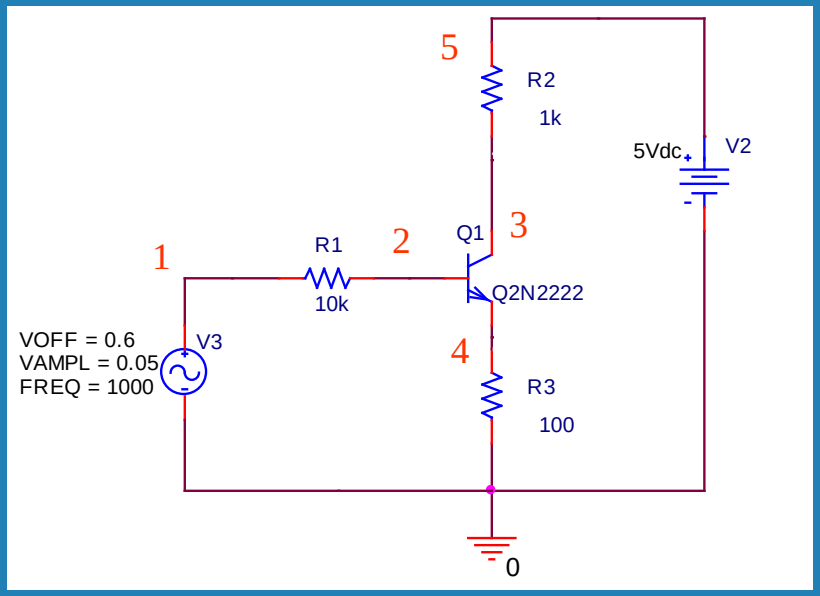


Voltage Regulation

With a Zener diode, V(7) is better regulated.

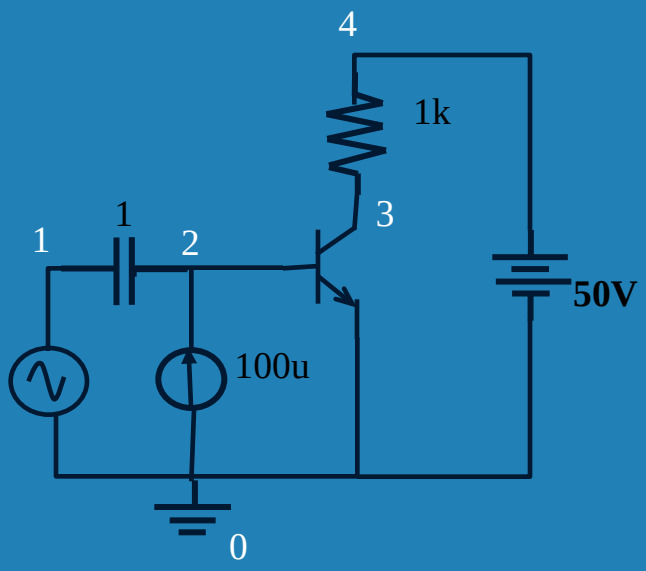


Transistor Circuit




```
* source ONE_TRANSISTOR
R_R1        1 2  10k
R_R2        3 5  1k
R_R3        0 4  100
V_V2        5 0 5Vdc
Q_Q1        3 2 4 Q2N2222
V_V3        1 0
+SIN 0.6 0.05 1000 0 0 0
```

Spice Netlist




```
BJT Noise Test
vcc 4 0 50
vin 1 0 ac
ccouple 1 2 1
ibias 0 2 100uA
rload 4 3 1k
q1 3 2 0 0 test

.model test npn kf=1e-20 af=1 bf=100 rb=10
.noise v(3) vin dec 10 10 100k 1
.end
```

Behavioral Model

```
VOLTAGE MULTIPLIER
V1  1  0  PWL(0  0  1MS 5V 3MS –5V 5MS 5V 6MS 0)
.PARAM K = 0.4
V2  2  0  SIN(0  5  250  0  0  0)
*MULTIPLIER MODEL
Em  3  0 VALUE = {K*V(1,0)*V(2,0)}
R0  3  0  100
.TRAN 0.02MS  6MS
.PROBE
.END
```

Table Extension

```
DIODE CIRCUIT
V1   1  0  DC  15V
R1  1  2  5K
R2  2  0  5K
R3  2  3  10K
R4  3  0  10K
GDIODE  3  4  TABLE  {V(3,4)} = (0  0)  (0.1  0.13E-11)
+ (0.2  1.8E-11)  (0.3  24.1E-11)  (0.4  0.31E-8)  (0.5  4.31E-8)
+ (0.6  58.7E-8)  (0.7  7.8E-6)
R5  4  0  10K
.DC  V1  15  15  1
.PRINT  DC  I(R5)
.END
```

Freq Extension

```
FILTER CHARACTERISTIC
VIN  1  0  AC  1  0
R1  1  0  1K
EFILTER  2  0  FREQ  {V(1,0)} = (1.0K, -14, 107)  (1.9K, -9.6, 90)  (2.5K, -5.9, 72)
+ (4.0K, -3.3, 55)  (6.3K, -1.6, 39)  (10K, -0.7, 26)  (15.8K, -0.3, 17)
+ (25K, -0.1, 11)  (40K, -0.05, 7)  (63K, -0.02, 4)  (100K, -0.008, 3)
R2  2  0  1K
.AC DEC 5  1000  1.0E5
.PROBE  V(2)  V(1)
.END
```

(FREQ, MAG_DB, PHASE)

Acknowledgement

- The examples in this tutorial are mostly taken from the textbook:

Robert Lamey, *The Illustrated Guide to Pspice*, Delmar Publishers Inc., 1995.